



AMDV040N060PSURH

Single N-channel Trench MOSFET 40V 6.0mΩ

FEATURES

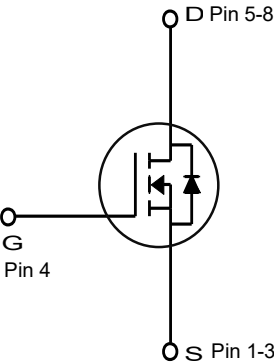
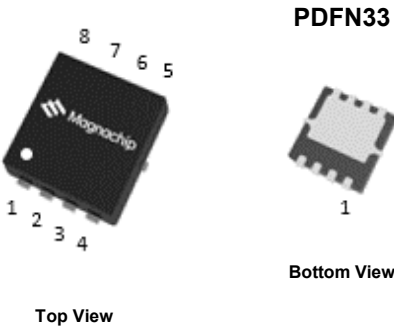
- Trench power MOSFET technology
- Single N-channel trench, Normal gate level
- Enhanced avalanche ruggedness
- 100% Avalanche tested
- Maximum 175°C junction temperature

PRODUCT VALIDATION

- Qualified according to AEC-Q101 Standard

KEY PERFORMANCE PARAMETERS

V_{DS}	40	V
$R_{DS(on), typ.}$	0.005	Ω
I_D	57	A
Q_g	12	nC
Junction temperature _{, max}	175	°C



RoHS Compliant
HALOGEN-FREE



ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
AMDV040N060PSURH	PDFN33	040N060	Tape & Reel	Halogen Free

<http://www.magnachip.com>

ABSOLUTE MAXIMUM RATINGS, at $T_C = 25^\circ\text{C}$, unless otherwise specified

Parameter		Symbol	Rating	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	
Drain current	$T_C=25^\circ\text{C}$ (Silicon Limited)	I_D	57	A
	$T_C=25^\circ\text{C}$ (Package Limited)		40	
	$T_C=100^\circ\text{C}$ (Silicon Limited)		40	
¹⁾ Pulsed drain current	$T_C=25^\circ\text{C}$, $t_P \leq 100 \mu\text{s}$	I_{DM}	149	
Total power dissipation	$T_C=25^\circ\text{C}$	P_{tot}	34	W
	$T_C=100^\circ\text{C}$		17	
²⁾ Avalanche energy, single pulse		E_{AS}	34	mJ
Operating and storage temperature		T_J, T_{stg}	- 55 ~ 175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Parameter	Symbol	Rating	Unit
Thermal resistance, junction - case	$R_{\theta JC}$	4.4	$^\circ\text{C/W}$
³⁾ Thermal resistance, junction - ambient	$R_{\theta JA}$	60	

ELECTRICAL CHARACTERISTICS (T_J = 25°C)**STATIC CHARACTERISTICS**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Drain-source breakdown voltage	V _{(BR)DSS}	40	-	-	V	V _{GS} =0 V, I _D =250 μA
Gate threshold voltage	V _{GS(th)}	2.25	-	3.75		V _{DS} =V _{GS} , I _D =65 μA
Zero gate voltage drain current	I _{DSS}	-	-	1	μA	V _{DS} =40 V, V _{GS} =0 V
Gate-source leakage current	I _{GSS}	-	-	± 100	nA	V _{GS} =±20 V, V _{DS} =0 V
Drain-source on-state resistance	R _{DS(on)}	-	5.00	6.00	mΩ	V _{GS} =10 V, I _D =15 A
		-	5.40	6.50		V _{GS} =8 V, I _D =15 A
⁴⁾ Gate resistance	R _g	-	1.6	-	Ω	f=1 MHz
⁴⁾ Transconductance	g _{fs}	-	40	-	S	V _{DS} =10 V, I _D =15 A

⁴⁾ DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Input capacitance	C _{iss}	-	857	-	pF	V _{GS} =0 V, V _{DS} =20 V, f=1 MHz
Output capacitance	C _{oss}	-	240	-		
Reverse transfer capacitance	C _{rss}	-	24	-		
Turn-on delay time	t _{d(on)}	-	13	-	ns	V _{DD} =20 V, V _{GS} =10 V, I _D =15 A, R _{G,ext} =3.5 Ω
Rise time	t _r	-	3	-		
Turn-off delay time	t _{d(off)}	-	22	-		
Fall time	t _f	-	4	-		

⁴⁾ GATE CHARGE CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Gate to source charge	Q _{gs}	-	2	-	nC	V _{DD} =20 V, I _D =15 A, V _{GS} =0 to 10 V
Gate charge at threshold	Q _{gs(th)}	-	2	-		
Gate to drain charge	Q _{gd}	-	2	-		
Switching charge	Q _{sw}	-	2	-		
Gate charge total	Q _g	-	13	-		
Gate plateau voltage	V _{plateau}	-	3.36	-	V	

SOURCE-DRAIN DIODE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
⁴⁾ Diode continuous forward current	I _S	-	-	40	A	-
⁴⁾ Diode pulse current	I _{S,pulse}	-	-	149		pulsed; t _p ≤ 100 μs
Diode forward voltage	V _{SD}	-	0.8	1.1	V	V _{GS} =0 V, I _F =15 A
⁴⁾ Reverse recovery time	t _{rr}	-	21	-	ns	I _F =15 A, di _F /dt=100 A/μs
⁴⁾ Reverse recovery charge	Q _{rr}	-	6	-	nC	

Notes

1. Pulse width limited by T_{Jmax}
2. Starting T_J=25°C, L=1mH, I_{AS}=8.3A, V_{DD}=36V, V_{GS}=10V
3. Surface mounted FR-4 board by JEDEC (jesd51-7)
4. The parameter is not subject to production testing - guaranteed by design

ELECTRICAL CHARACTERISTICS DIAGRAMS

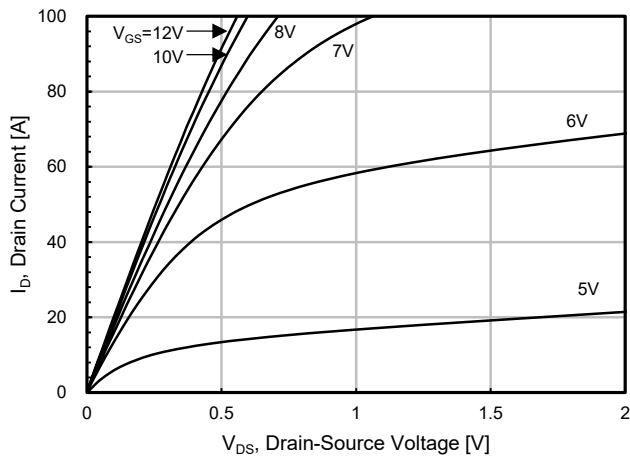


Fig. 1. Typ. Output Characteristics

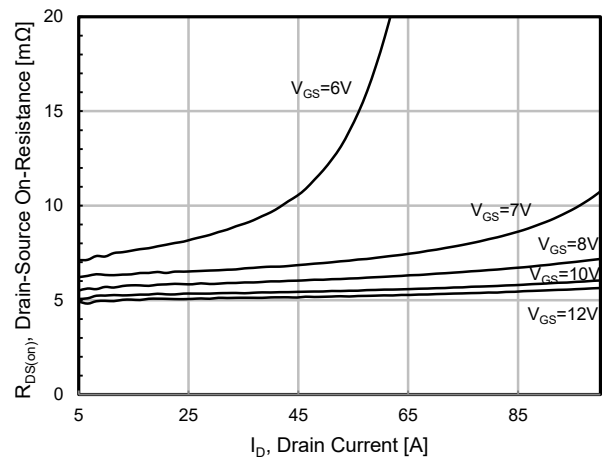


Fig. 2. Typ. Drain-Source On-Resistance

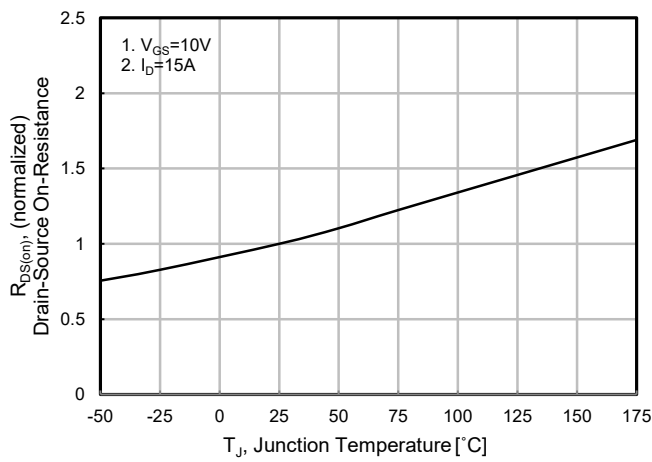


Fig. 3. On-Resistance vs. Junction Temperature

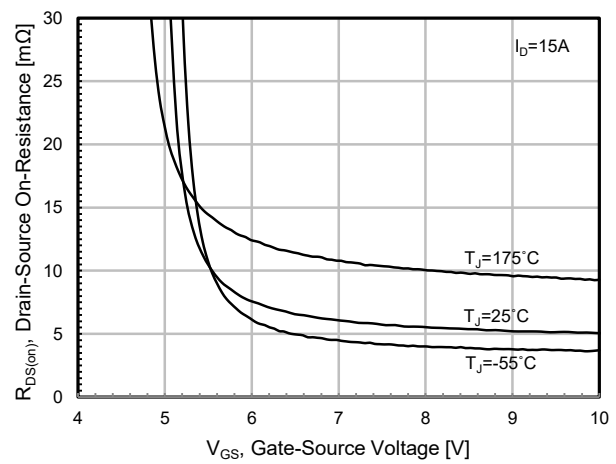


Fig. 4. On-Resistance vs. Gate-Source Voltage

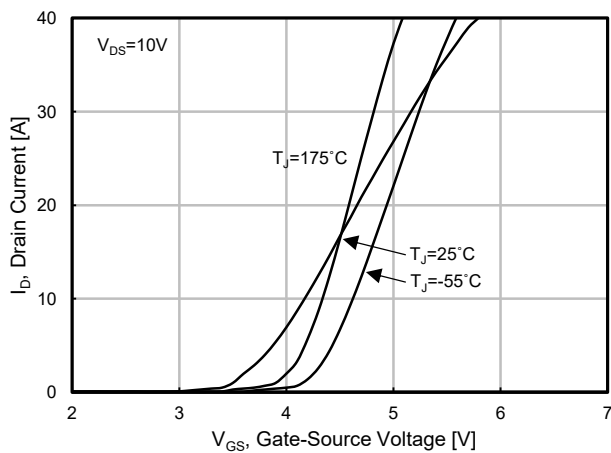


Fig. 5. Transfer Characteristics

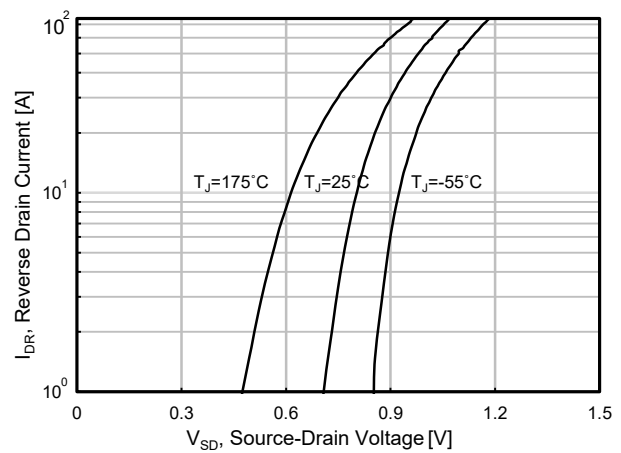


Fig. 6. Forward Characteristics of Reverse Diode

ELECTRICAL CHARACTERISTICS DIAGRAMS

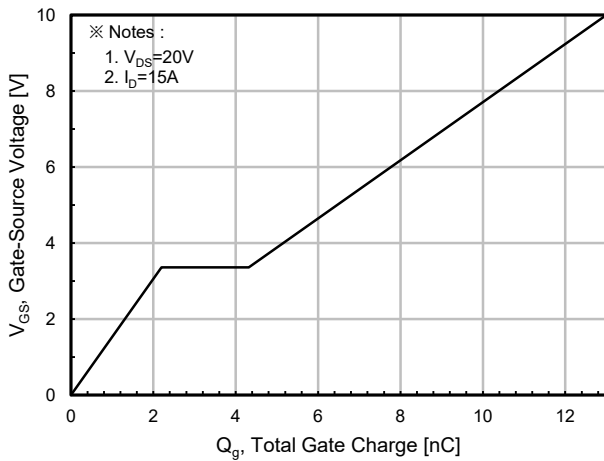


Fig. 7. Typ. Gate Charge

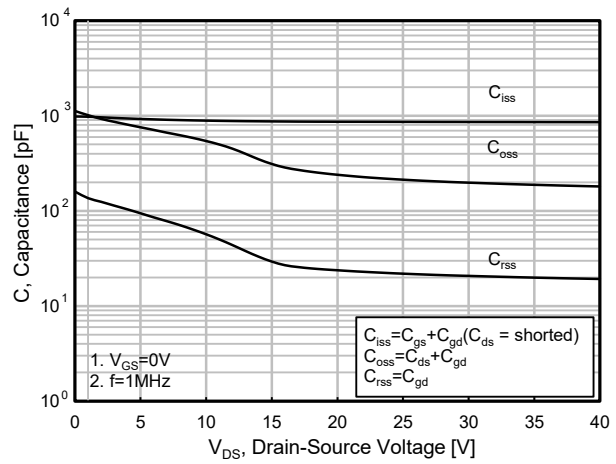


Fig. 8. Typ. Capacitance

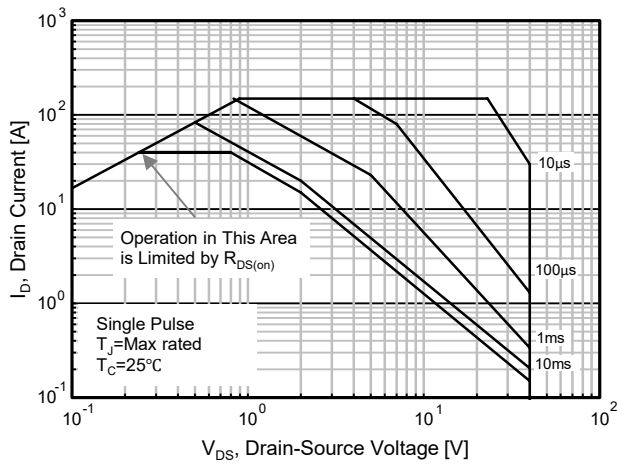


Fig. 9. Safe Operating Area

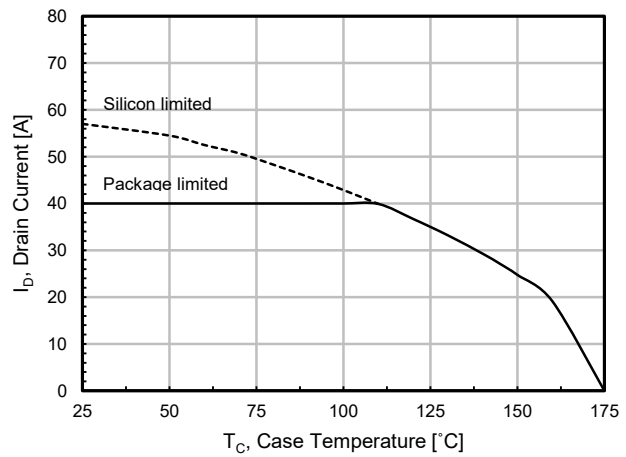


Fig. 10. Drain Current vs. Temperature

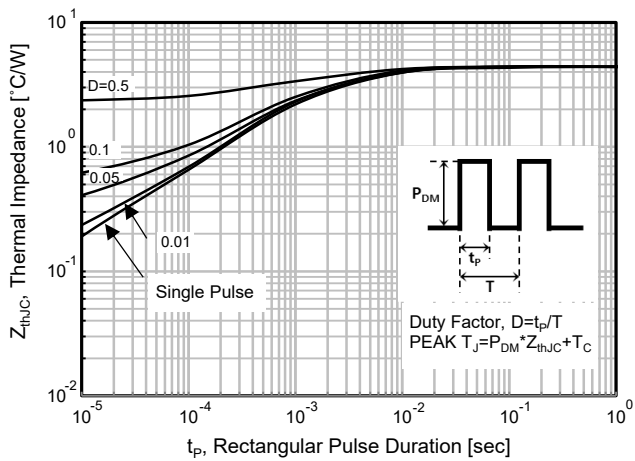
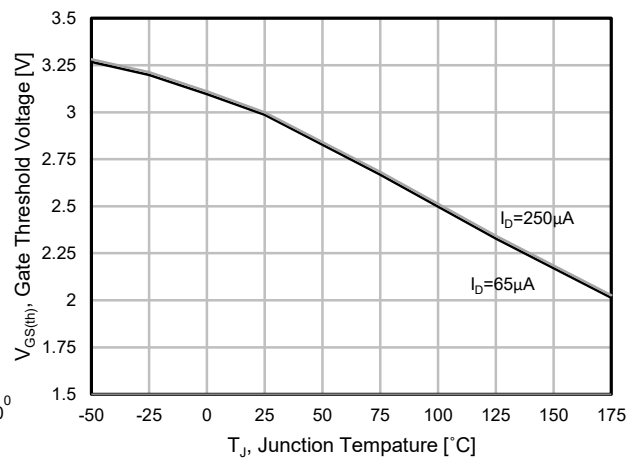


Fig. 11. Transient Thermal Impedance

Fig. 12. $V_{GS(th)}$ Variation with Temperature

ELECTRICAL CHARACTERISTICS DIAGRAMS

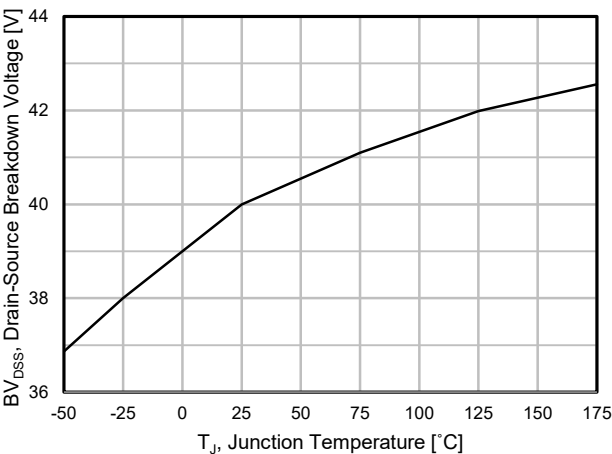


Fig. 13. BV_{DSS} Variation with Temperature

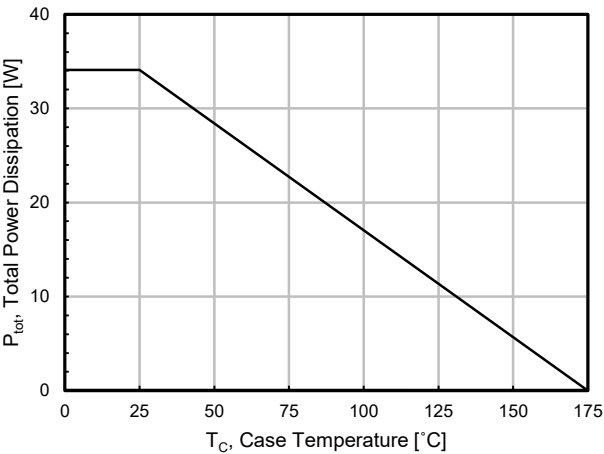
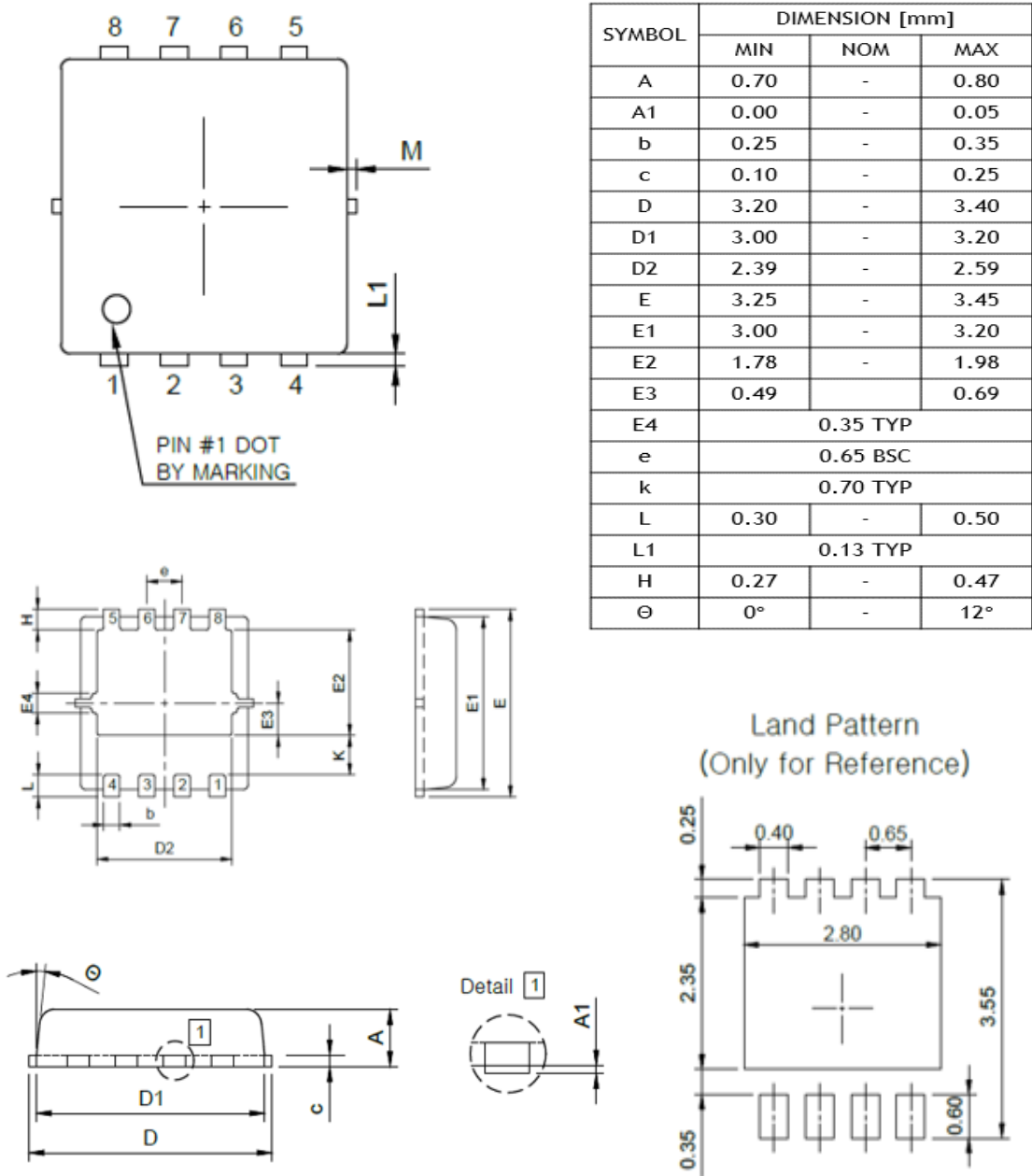


Fig. 14. Power Dissipation

Package Outlines

PDFN33



Notes
Package body size, length and width do not include mold flash, protrusions and gate burrs.

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