AMDU040N035LVRH

Single N-channel Trench MOSFET 40V 3.5mΩ

FEATURES

- Trench power MOSFET technology
- Single N-channel trench, logic level
- Enhanced avalanche ruggedness
- 100% Avalanche tested
- Maximum 175°C junction temperature

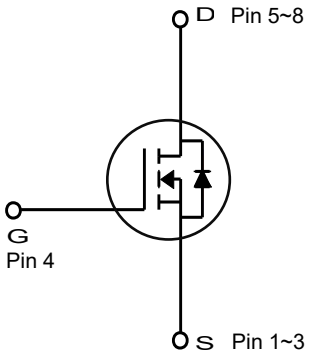
Top View

PDFN56

Bottom View

PRODUCT VALIDATION

- Qualified according to AEC-Q101 Standard



KEY PERFORMANCE PARAMETERS

V_{DS}	40	V
$R_{DS(on),\ typ.}$	2.6	mΩ
I_D	106	A
Qg	24	nC
Junction temperature, max	175	°C

RoHS Compliant
HALOGEN-FREE

AUTOMOTIVE

ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
AMDU040N035LVRH	PDFN56	040N035L	Tape & Reel	Halogen Free

http://www.magnachip.com/

ABSOLUTE MAXIMUM RATINGS (T_C = 25℃, unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	
Drain current	Tc=25°C (Silicon Limited)	I_D	106	A
	Tc=25°C (Package Limited)		100	
	Tc=100°C (Silicon Limited)		75	
1) Pulsed drain current	Tc=25℃	I_{DM}	400	
Total power dissipation	Tc=25℃	P_{tot}	71	W
	Tc=100℃		35	
2) Avalanche energy, single pulse		E_{AS}	88	mJ
Operating and storage temperature		T_j, T_{stg}	- 55 ~ 175	℃

THERMAL CHARACTERISTICS

Parameter	Symbol	Rating	Unit
3) Thermal resistance, junction - case	$R_{\theta JC}$	2.1	°C/W
3) Thermal resistance, junction - ambient	$R_{\theta JA}$	60	

ELECTRICAL CHARACTERISTICS (T_J = 25℃, unless otherwise specified)

STATIC CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=250 μA
Gate threshold voltage	$V_{GS(th)}$	1.1	-	2.5	V	V_{DS}=V_{GS}, I_D=250 μA
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=40 V, V_{GS}=0 V
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	V_{GS}=±20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	4.0	5.8	mΩ	V_{GS}=4.5 V, I_D=50 A
		-	2.6	3.5		V_{GS}=10V, I_D=50 A
[4] Gate resistance	R_G	-	3.0	-	Ω	f=1MHz
[4] Transconductance	g_{fs}	-	85	-	S	V_{DS}=10 V, I_D=50 A

[4] DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Input capacitance	C_{iss}	-	1729	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance	C_{oss}	-	458	-		
Reverse transfer capacitance	C_{rss}	-	37	-		
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=3Ω
Rise time	t_r	-	6	-		
Turn-off delay time	$t_{d(off)}$	-	38	-		
Fall time	t_f	-	10	-		

[4] GATE CHARGE CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Gate to source charge	Q_{gs}	-	6	-	nC	V_{DD}=32 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{gs(th)}$	-	2	-		
Gate to drain charge	Q_{gd}	-	4	-		
Switching charge	Q_{sw}	-	8	-		
Gate charge total	Q_g	-	24	-		
Gate plateau voltage	$V_{plateau}$	-	3.7	-	V	

SOURCE-DRAIN DIODE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
[4] Diode continuous forward current	I_S	-	-	100	A	-
[4] Diode pulse current	$I_{S,pulse}$	-	-	400		pulsed; $t_p \leq 10$ μs
Diode forward voltage	V_{SD}	-	0.8	1.1	V	V_{GS}=0 V, I_F=20 A
[4] Reverse recovery time	t_{rr}	-	24	-	ns	I_F=50 A, di_F/dt=100 A/μs
[4] Reverse recovery charge	Q_{rr}	-	18	-	nC	

Notes

1. Pulse width limited by Tjmax
2. Starting T_J=25°C, L=1mH, I_{AS}=13.3A, V_{DD}=36V, V_{GS}=10V
3. Surface mounted FR-4 board by JEDEC (jesd51-7)
4. The parameter is not subject to production testing - guaranteed by design.

Electrical Characteristics Diagrams (T_J = 25 ℃, unless otherwise specified)

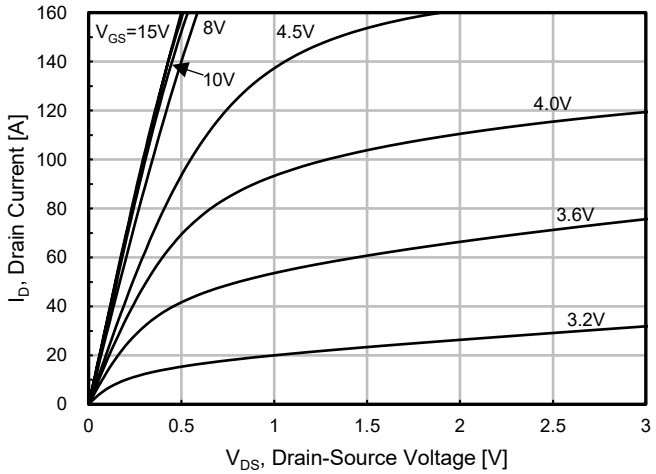


Fig. 1. Typ. Output Characteristics

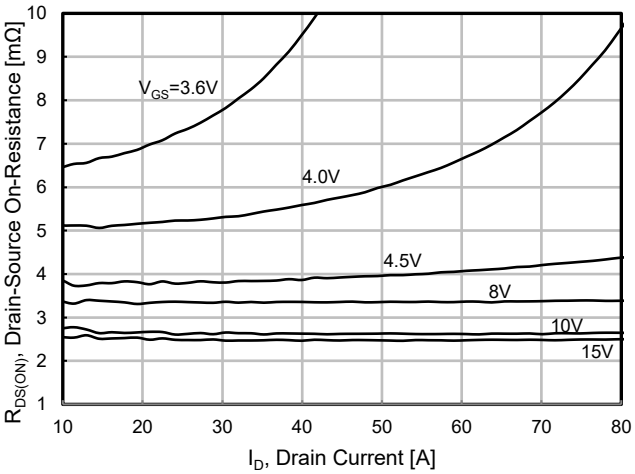


Fig. 2. Typ. Drain to Source On-Resistance

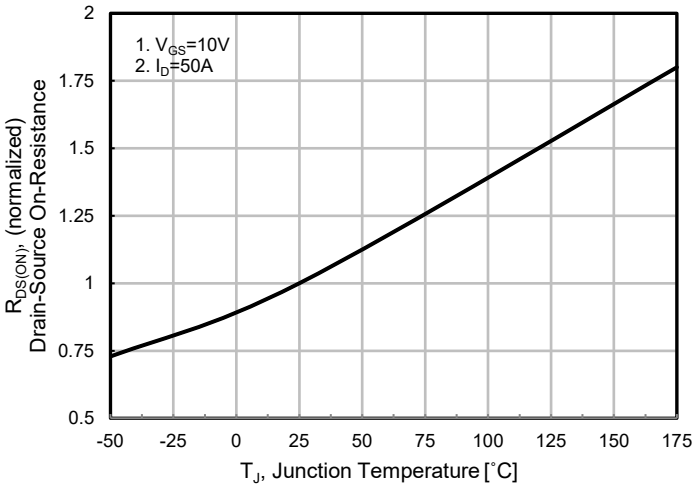


Fig. 3. On-Resistance vs. Junction Temperature

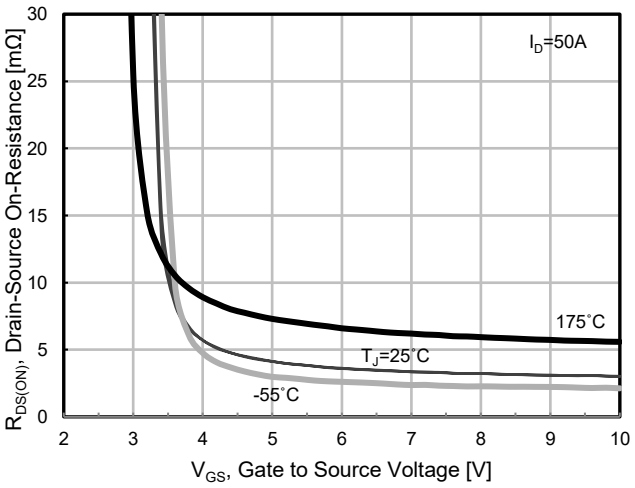


Fig. 4. On-Resistance vs. Gate to source Voltage

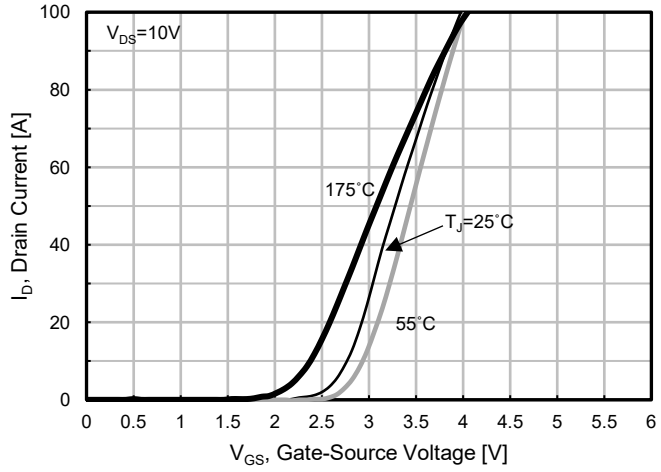


Fig. 5. Typ. Transfer Characteristics

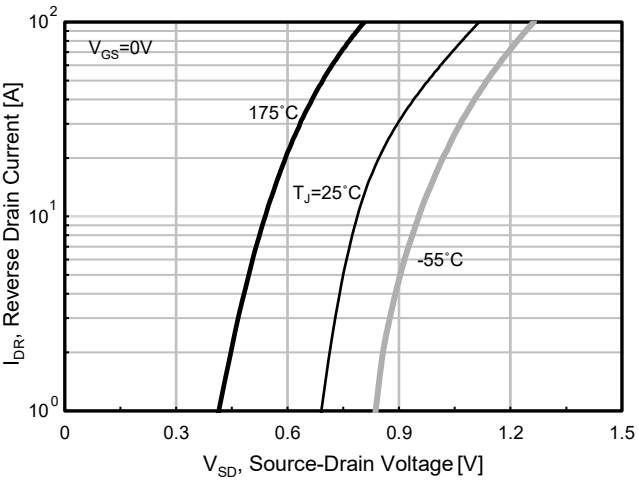


Fig. 6. Forward Characteristics of Reverse Diode

Electrical Characteristics Diagrams (T_J = 25 ℃, unless otherwise specified)

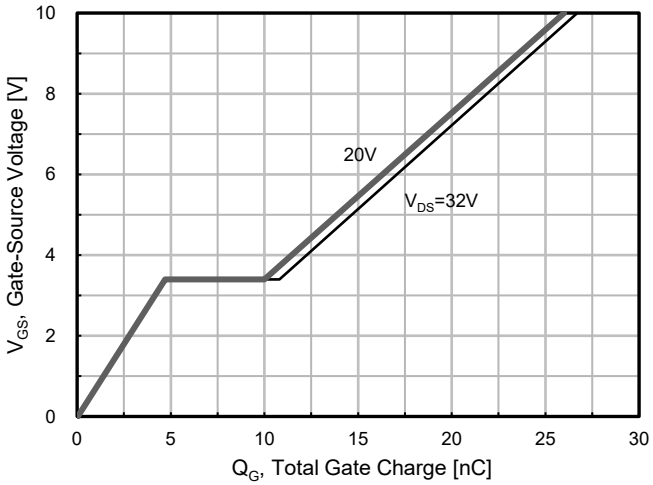


Fig. 7. Typ. Gate Charge

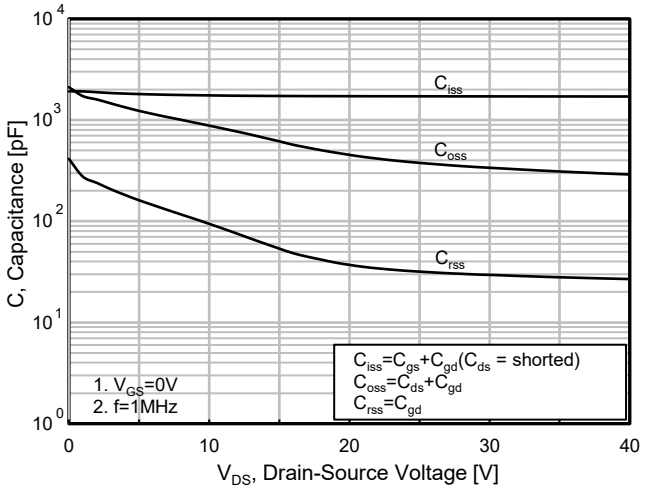


Fig. 8. Typ. Capacitance

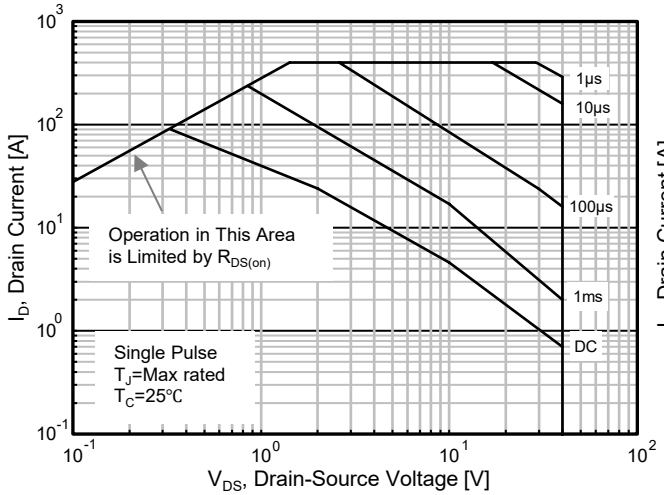


Fig. 9. Safe Operating Area

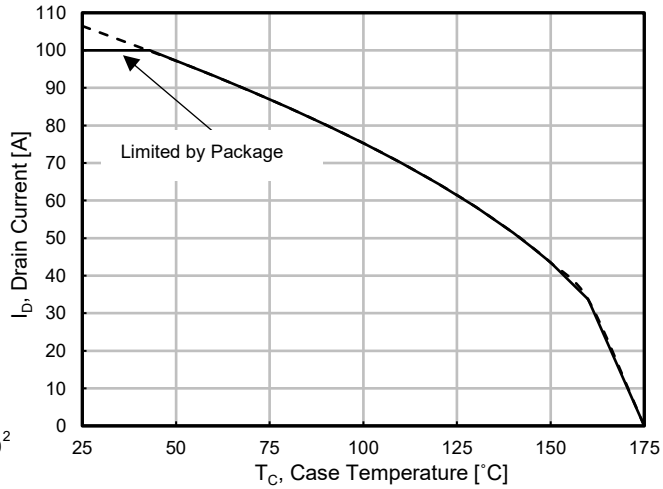


Fig. 10. Drain Current vs. Temperature

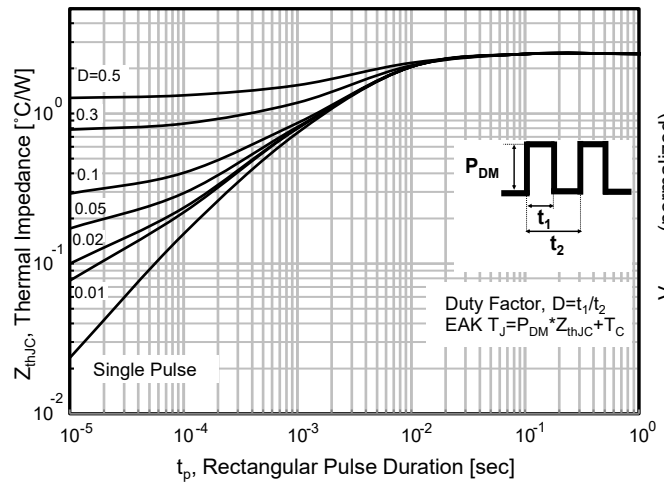


Fig. 11. Transient Thermal Impedance

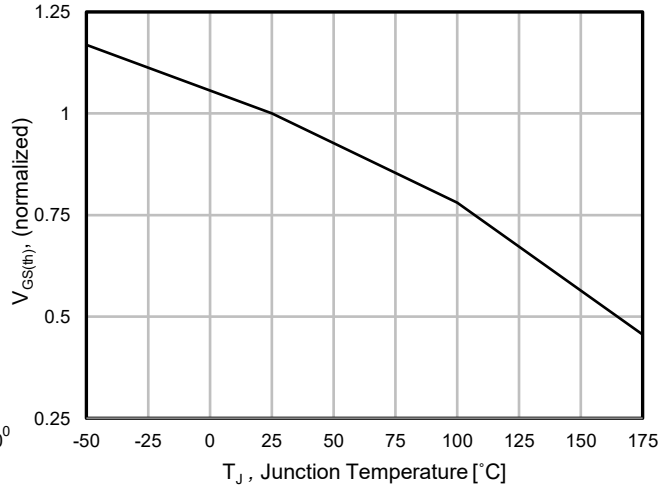


Fig. 12. VGS(th) Variation with Temperature (Normalized)

Electrical Characteristics Diagrams (T_J = 25 ℃, unless otherwise specified)

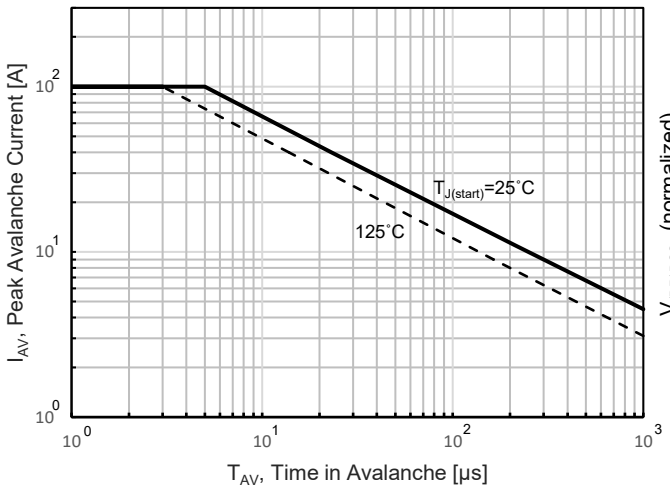


Fig. 13. Avalanche Characteristics

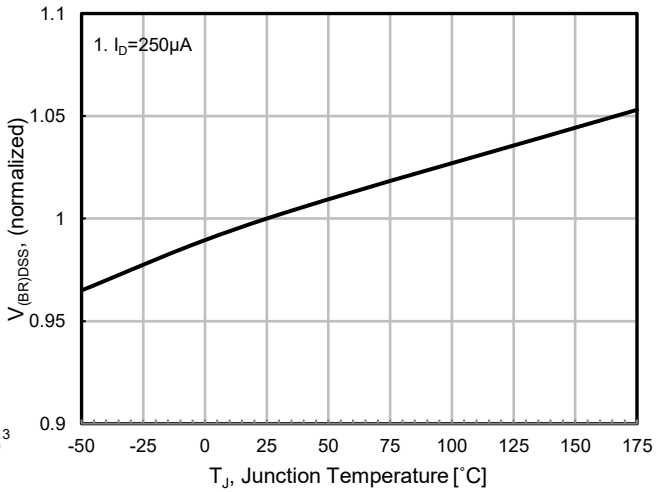


Fig. 14. V(BR)DSS Variation with Temperature (Normalized)

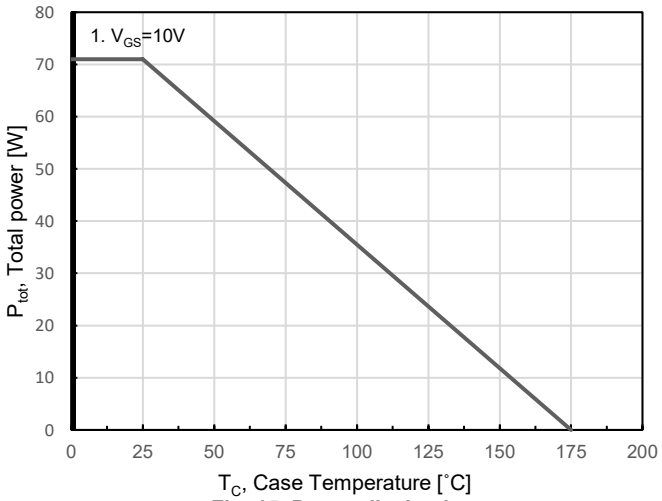
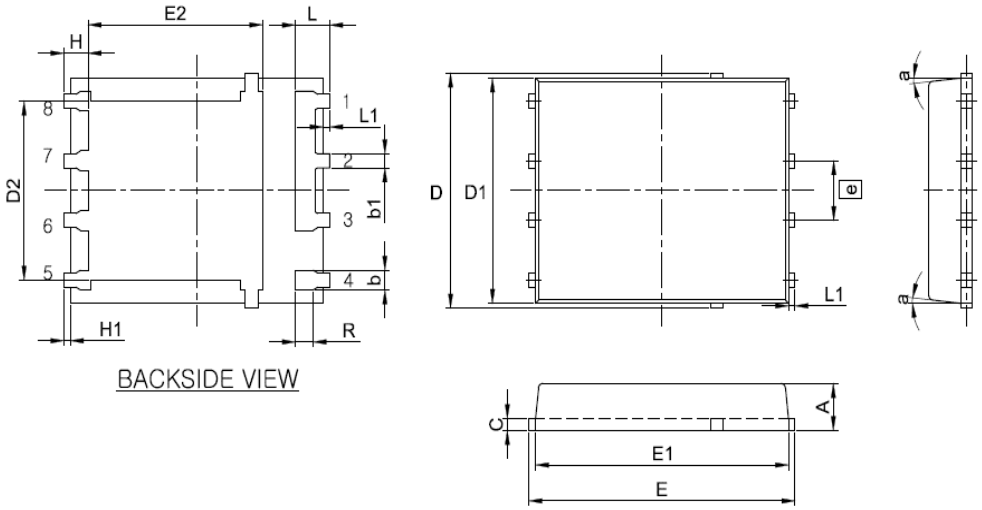


Fig. 15. Power dissipation

Package Outlines

PDFN56



Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.90	-	1.10
b	0.33	-	0.49
b1	0.26	-	1.36
C	0.25 BSC		
D	5.15 BSC		
D1	5.00 BSC		
D2	3.70	-	3.90
E	6.15 BSC		
E1	6.00 BSC		
E2	3.56	-	3.76
e	1.27 BSC		
H	0.50	-	0.71
H1	0.03	-	0.13
L	0.74	-	0.84
L1	0.03	-	0.13
R	0.48	-	0.58
a	0°	-	12°

Notes

Package body size, length and width do not include mold flash, protrusions and gate burrs.

DISCLAIMER :

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.