



AMDU040N033VRH

Single N-channel Trench MOSFET 40V 3.3mΩ 100A

FEATURES

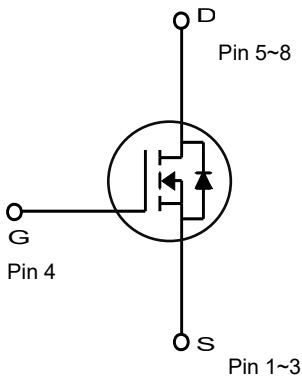
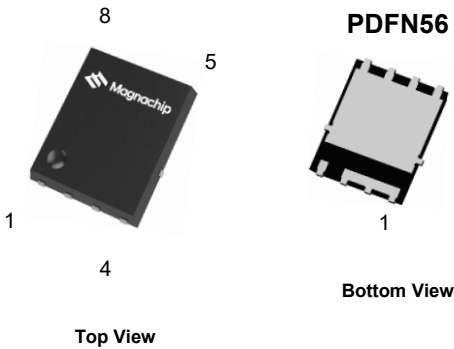
- Trench power MOSFET technology
- Single N-channel trench, normal level
- Enhanced avalanche ruggedness
- 100% Avalanche tested
- Maximum 175°C junction temperature

PRODUCT VALIDATION

- Qualified according to AEC-Q101 Standard

KEY PERFORMANCE PARAMETERS

V_{DS}	40	V
$R_{DS(on), typ.}$	0.0025	Ω
I_D	100	A
Q_g	27	nC
Junction temperature _{, max}	175	°C



RoHS Compliant
HALOGEN-FREE



ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
AMDU040N033VRH	PDFN56	040N033	Tape & Reel	Halogen Free

<http://www.magnachip.com/>

ABSOLUTE MAXIMUM RATINGS, at $T_c = 25^{\circ}\text{C}$, unless otherwise specified

PARAMETER		SYMBOL	RATING	UNIT
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	
Drain current	$T_c=25^{\circ}\text{C}$ (Silicon Limited)	I_D	110	A
	$T_c=25^{\circ}\text{C}$ (Package Limited)		100	
	$T_c=100^{\circ}\text{C}$ (Silicon Limited)		78	
¹⁾ Pulsed drain current	$T_c=25^{\circ}\text{C}$	I_{DM}	400	
Total power dissipation	$T_c=25^{\circ}\text{C}$	P_{tot}	73	W
	$T_c=100^{\circ}\text{C}$		36	
²⁾ Avalanche energy, single pulse		E_{AS}	111	mJ
Operating and storage temperature		T_j, T_{stg}	- 55 ~ 175	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATING	UNIT
Thermal resistance, junction - case	$R_{\theta JC}$	2.05	$^{\circ}\text{C}/\text{W}$
³⁾ Thermal resistance, junction - ambient	$R_{\theta JA}$	60	

ELECTRICAL CHARACTERISTICS (T_J = 25°C)**STATIC CHARACTERISTICS**

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Drain-source breakdown voltage	V _{(BR)DSS}	40	-	-	V	V _{GS} =0 V, I _D =250 μA
Gate threshold voltage	V _{GS(th)}	2.25	-	3.75	V	V _{DS} =V _{GS} , I _D =250 μA
Zero gate voltage drain current	I _{DSS}	-	-	1	μA	V _{DS} =40 V, V _{GS} =0 V
Gate-source leakage current	I _{GSS}	-	-	± 100	nA	V _{GS} =±20 V, V _{DS} =0 V
Drain-source on-state resistance	R _{DS(on)}	-	3.0	4.0	mΩ	V _{GS} =7 V, I _D =20 A
		-	2.5	3.3		V _{GS} =10V, I _D =20 A
⁴⁾ Gate resistance	R _G	-	3.5	-	Ω	f=1 MHz
⁴⁾ Transconductance	g _{fs}	-	86	-	S	V _{DS} =10 V, I _D =50 A

⁴⁾ DYNAMIC CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Input capacitance	C _{iss}		1995	-	pF	V _{GS} =0 V, V _{DS} =20 V, f=1 MHz
Output capacitance	C _{oss}		642	-		
Reverse transfer capacitance	C _{rss}		56	-		
Turn-on delay time	t _{d(on)}		16	-	ns	V _{DD} =20 V, V _{GS} =10 V, I _D =50 A, R _{G,ext} =3 Ω
Rise time	t _r		10	-		
Turn-off delay time	t _{d(off)}		34	-		
Fall time	t _f		12	-		

⁴⁾ GATE CHARGE CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Gate to source charge	Q _{gs}		8	-	nC	V _{DD} =32 V, I _D =50 A, V _{GS} =0 to 10 V
Gate charge at threshold	Q _{gs(th)}		5	-		
Gate to drain charge	Q _{gd}		6	-		
Switching charge	Q _{sw}		9	-		
Gate charge total	Q _g		27	-		
Gate plateau voltage	V _{plateau}		4.8	-	V	

SOURCE-DRAIN DIODE

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
⁴⁾ Diode continuous forward current	I _S	-	-	100	A	-
⁴⁾ Diode pulse current	I _{S,pulse}	-	-	400		pulsed; t _p ≤ 10 μs
Diode forward voltage	V _{SD}	-	0.8	1.1	V	V _{GS} =0 V, I _F =20 A
⁴⁾ Reverse recovery time	t _{rr}	-	57	-	ns	I _F =50 A, di _F /dt=100 A/μs
⁴⁾ Reverse recovery charge	Q _{rr}	-	83	-	nC	

Notes

- Pulse width limited by T_{Jmax}
- Starting T_J=25°C, L=1mH, I_{AS}=14.9A, V_{DD}=36V, V_{GS}=10V
- Surface mounted FR-4 board by JEDEC (jesd51-7)
- The parameter is not subject to production testing - guaranteed by design.

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 °C, unless otherwise noted)

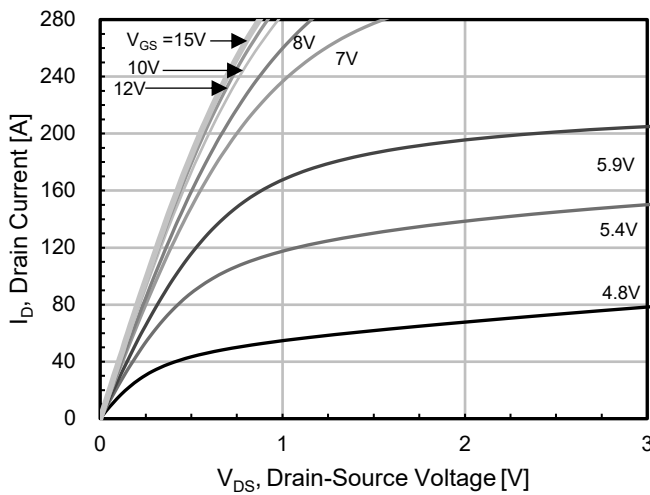


Fig. 1. Typ. Output Characteristics

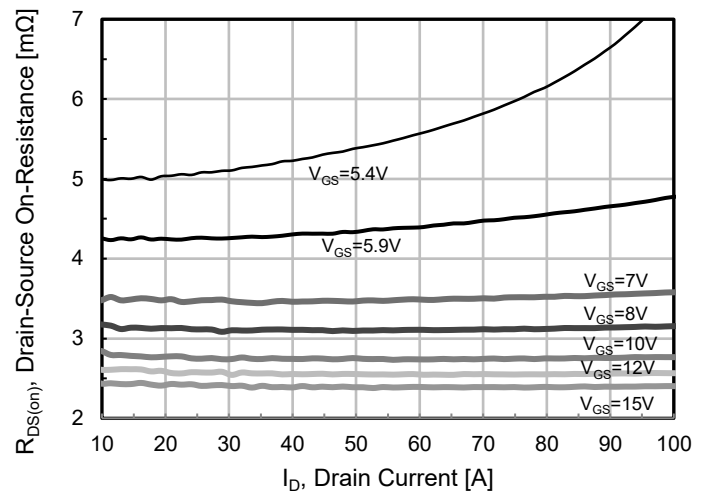


Fig. 2. Typ. Drain to Source On-Resistance

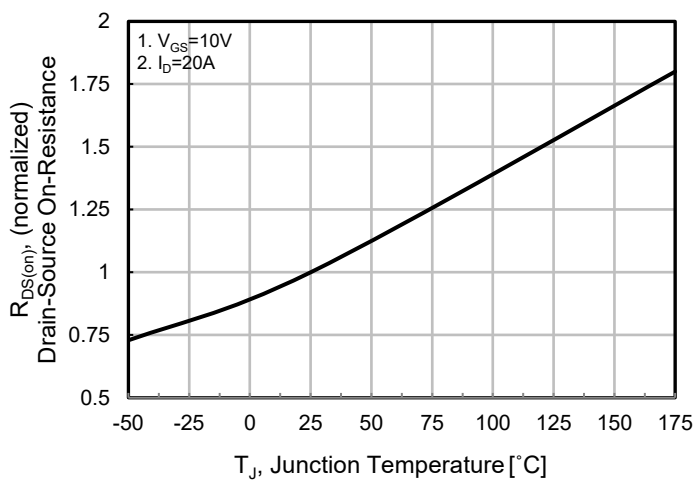


Fig. 3. On-Resistance vs. Junction Temperature

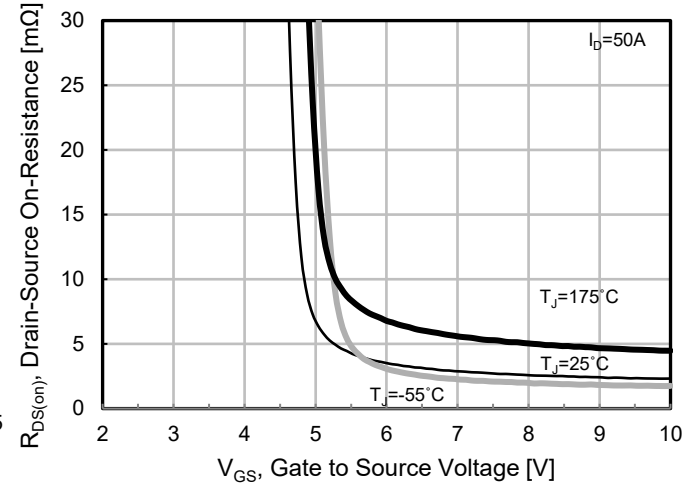


Fig. 4. On-Resistance vs. Gate to Source Voltage

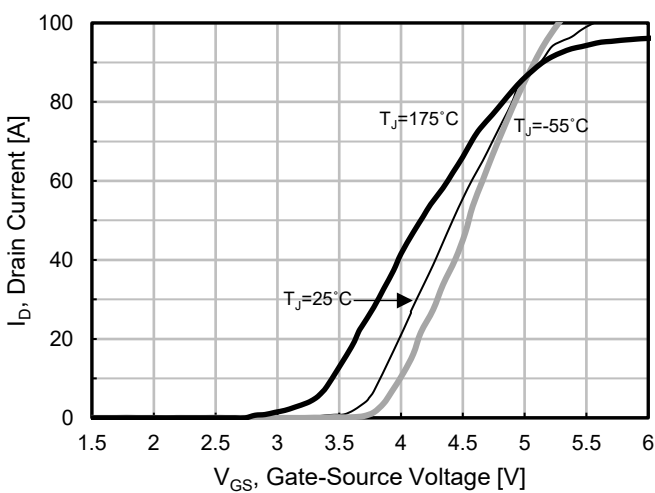


Fig. 5. Typ. Transfer Characteristics

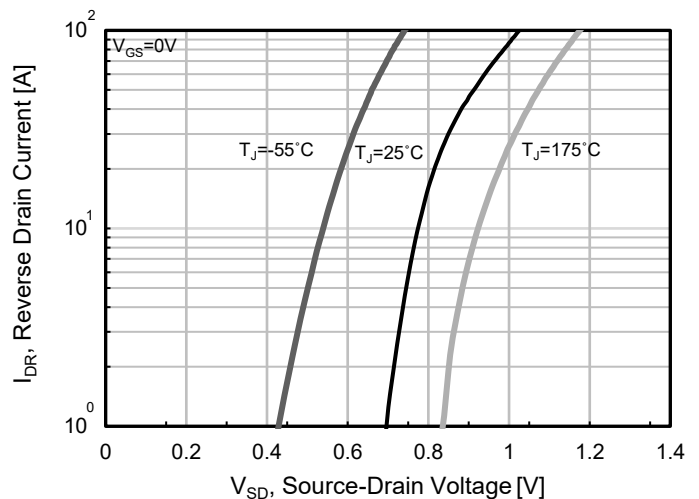


Fig. 6. Forward Characteristics of Reverse Diode

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 °C, unless otherwise noted)

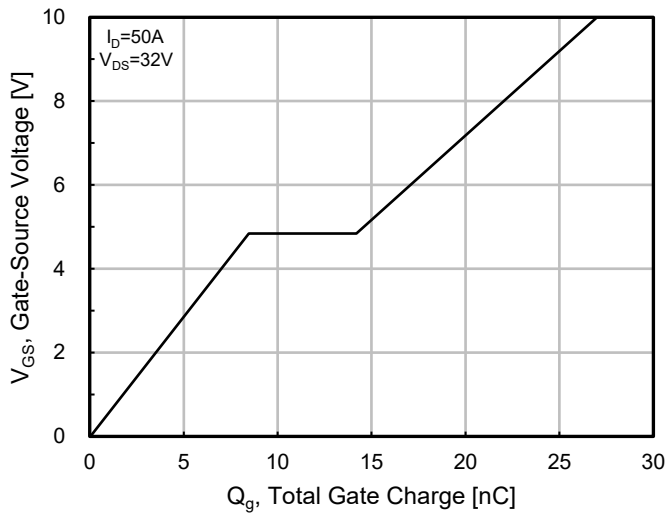


Fig. 7. Typ. Gate Charge

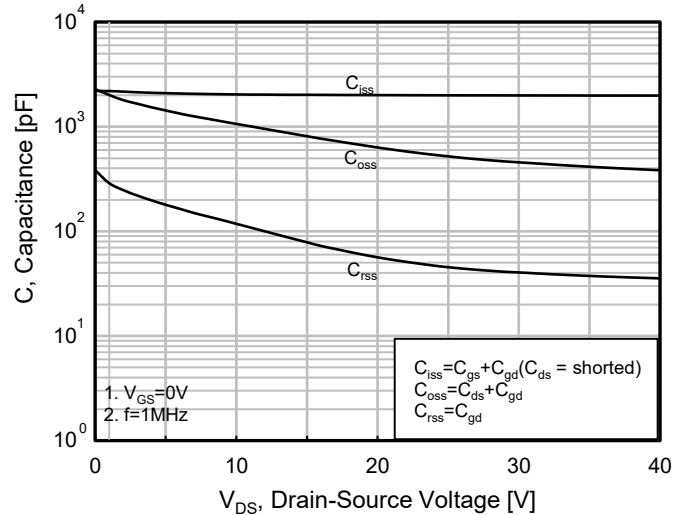


Fig. 8. Typ. Capacitances

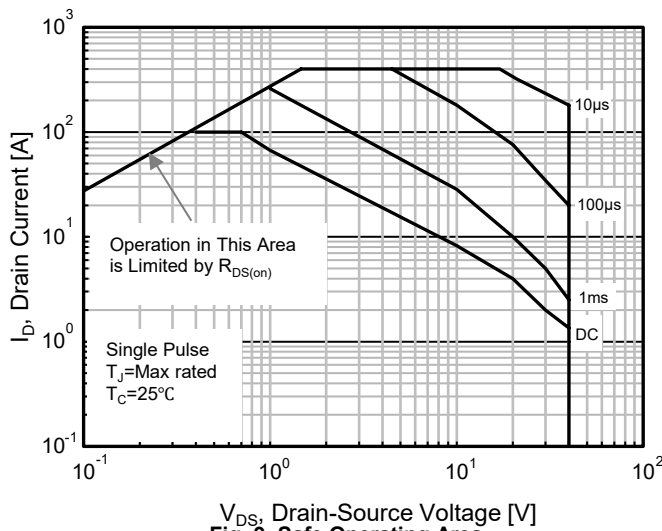


Fig. 9. Safe Operating Area

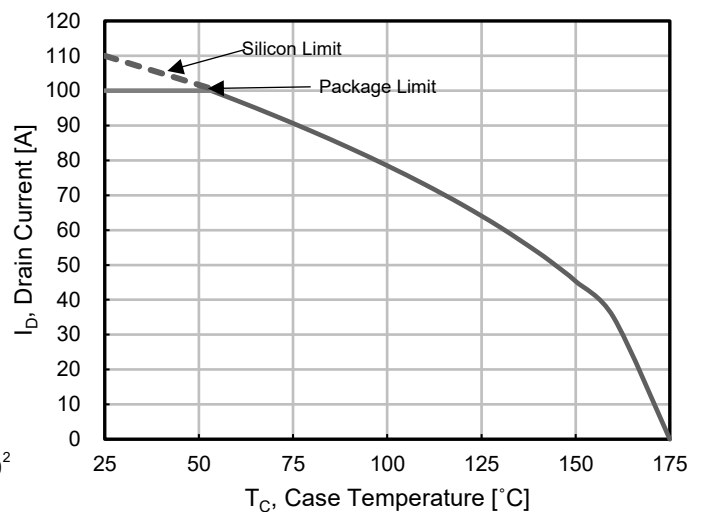


Fig. 10. Drain Current vs. Temperature

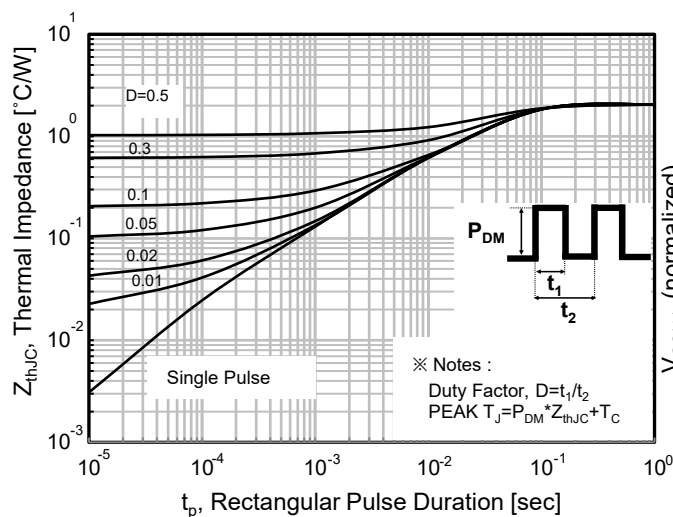
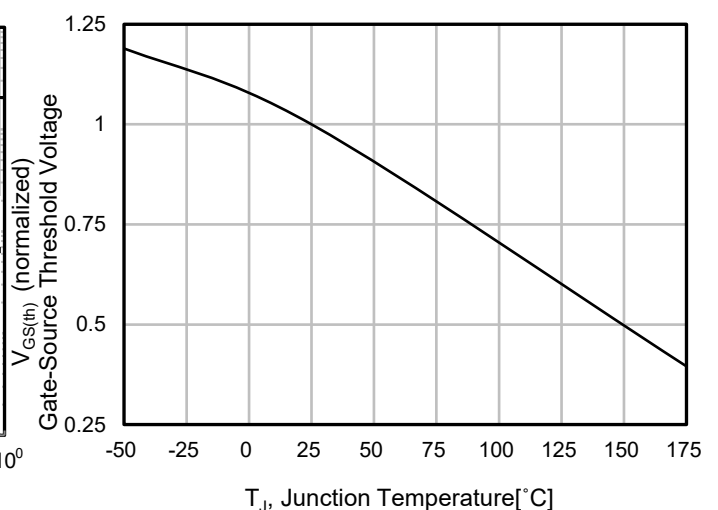


Fig. 11. Transient Thermal Impedance

Fig. 12. $V_{GS(th)}$ Variation with Temperature (Normalized)

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 °C, unless otherwise noted)

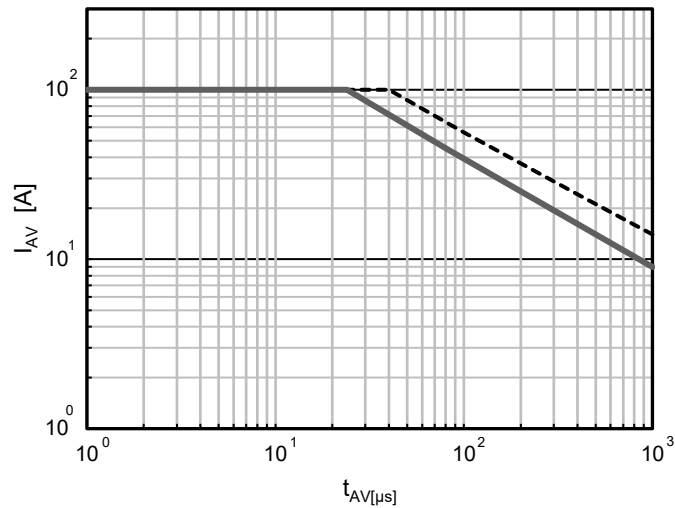


Fig. 13. Avalanche Characteristics

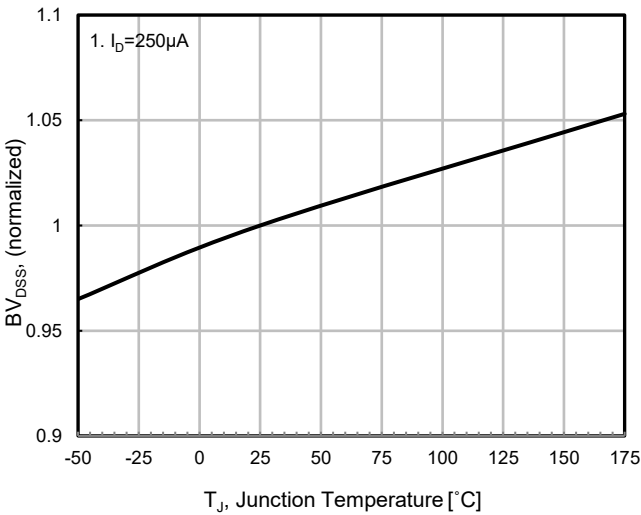


Fig. 14. BV_{DS} Variation with Temperature (Normalized)

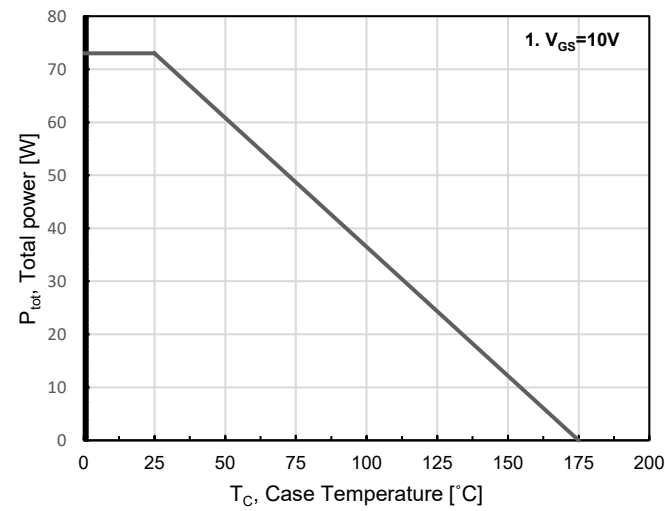
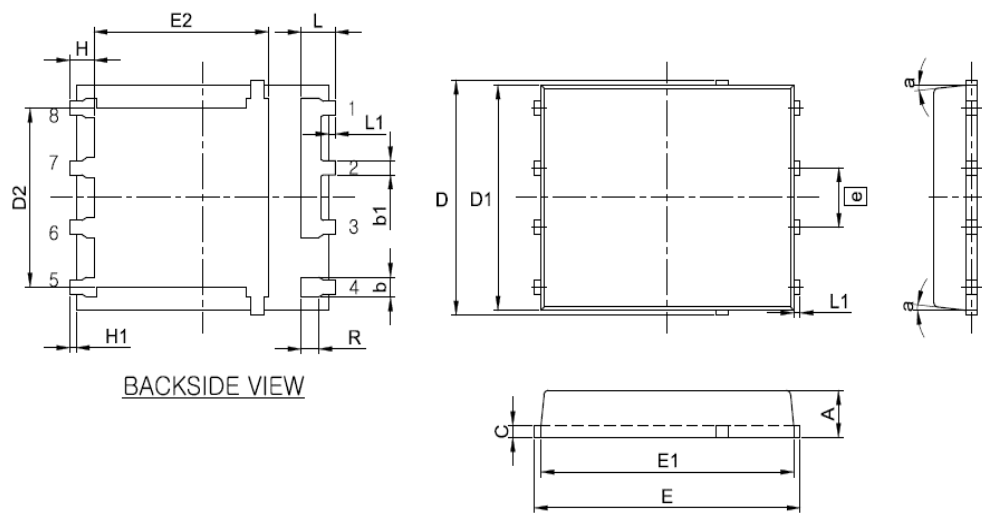


Fig. 15. Power dissipation

Package Outlines

PDFN56



Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.90	–	1.10
b	0.33	–	0.49
b1	0.26	–	1.36
C	0.25 BSC		
D	5.15 BSC		
D1	5.00 BSC		
D2	3.70	–	3.90
E	6.15 BSC		
E1	6.00 BSC		
E2	3.56	–	3.76
e	1.27 BSC		
H	0.50	–	0.71
H1	0.03	–	0.13
L	0.74	–	0.84
L1	0.03	–	0.13
R	0.48	–	0.58
a	0°	–	12°

Notes

Package body size, length and width do not include mold flash, protrusions and gate burrs.

DISCLAIMER :

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

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