RoHS Compliant

MagnaChip

MDW1304E

Common-Drain Dual N-Channel Trench MOSFET 24V

General Description

The MDW1304E uses advanced MagnaChip's MOSFET Technology, which provides high performance in on-state resistance, high switching performance and excellent reliability. Excellent low $R_{DS(ON)}$, low gate charge operation and operation for Battery Application.

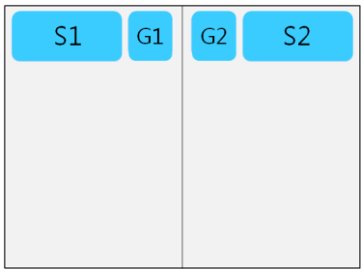
Features

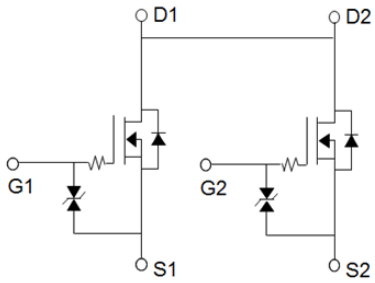
- V_{DS} = 24V
- Drain-Source ON Resistance;
  $R_{DS(ON)}$ < 40mΩ @ V_{GS} = 3.0V
  $R_{DS\ (ON)}$ < 34mΩ @ V_{GS} = 3.9V

Applications

- Portable Battery Protection Module
- Wearable Device Protection Module

Bottom View





Electrical Characteristics (T_A=25°C)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 500μA, V_{GS} = 0V	24	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1mA	0.5	1.0	1.5	
Drain Cut-Off Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V	-	-	1.0	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0V	-	-	10	μA
Drain-Source Resistance	$R_{DS(ON)}$	V_{GS} = 3.0V, I_D = 5.0A	-	33	40	mΩ
		V_{GS} = 3.9V, I_D = 5.0A	-	28	34	

Mechanical Data

Contents	Configuration
Passivation	TEOS (3,000 Å) - Nitride (6,000 Å)
Back Metal Composition (Thickness)	NiV (3,000 Å) – Ag (1,500 Å)
Front Metal Composition (Thickness)	Al (45,000 Å)
Die Dimension (with S/L)	1,240 um x 845 um
Gate Pad Dimension	120 um x 120 um
Wafer Diameter	200 mm, with 100 flat
Wafer Thickness	145 um
Scribe lane width	60 um

Electrical Characteristics (T_A =25ºC unless otherwise noted)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
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Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1mA	0.5	1.0	1.5	
Drain Cut-Off Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V	-	-	1.0	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0V	-	-	10	μA
Drain-Source Resistance Note 2	$R_{DS(ON)}$	V_{GS} = 3.0V, I_D = 5.0A	-	33	40	mΩ
		V_{GS} = 3.9V, I_D = 5.0A	-	28	34	
Forward Transconductance	g_{fs}	V_{DS} = 5V, I_D = 5A	-	9.5	-	S
Dynamic Characteristics Note 3						
Total Gate Charge	Q_g	V_{DS} = 12V, I_D = 5.0A, V_{GS} = 4.5V, I_G = 1mA	-	10.3	-	nC
Gate-Source Charge	Q_{gs}		-	3.9	-	
Gate-Drain Charge	Q_{gd}		-	3.9	-	
Input Capacitance	C_{iss}	V_{DS} = 12V, V_{GS} = 0V, f = 1MHz	-	525	-	pF
Reverse Transfer Capacitance	C_{rss}		-	195	-	
Output Capacitance	C_{oss}		-	223	-	
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 4.5V, V_{DS} = 12V, I_D = 5A, R_G = 6 Ω	-	0.08	-	us
Rise Time	t_r		-	2.2	-	
Turn-Off Delay Time	$t_{d(off)}$		-	0.6	-	
Fall Time	t_f		-	0.4	-	
Drain-Source Body Diode Characteristics Note 3						
Source-Drain Diode Forward Voltage	V_{SD}	I_S = 3.0A, V_{GS} = 0V	-	0.75	1.0	V

Notes :

1. The device current rating is derived from its thermal resistance and from the number and diameter of bonding wires.

   The testing current at wafer level is set only for ease of testing. Actual package current ratings can be much higher.

2. $R_{DS(ON)}$ is Single MOS . In this case, $R_{DS(ON)}$ is $R_{SS(ON)}$ / 2

3. Dynamic Characteristics and Drain-Source Body Diode Characteristics are tested on SOIC-8L Package.

Characteristic Graph

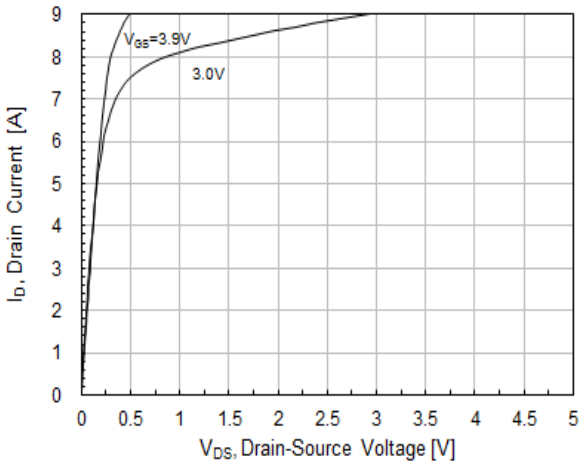


Fig.1 On-Region Characteristics

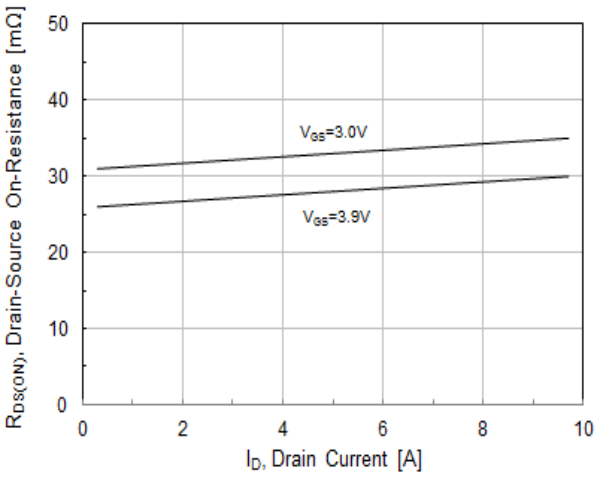


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

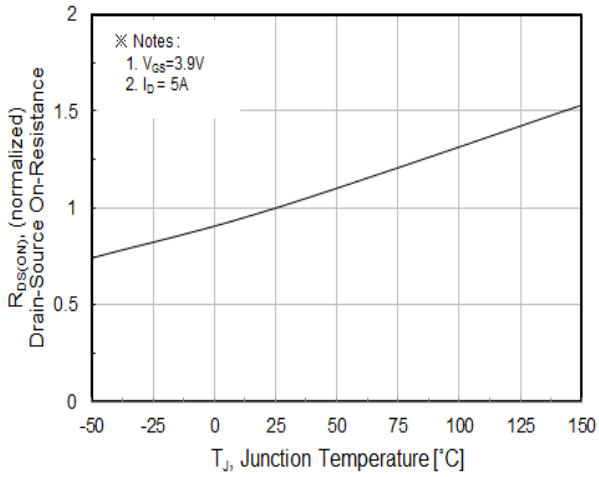


Fig.3 On-Resistance Variation with Temperature

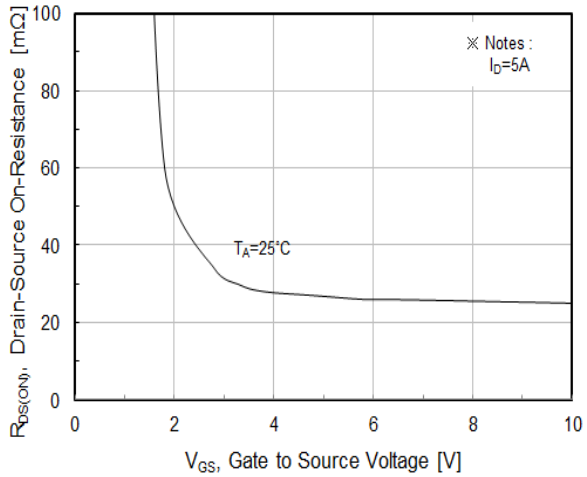


Fig.4 On-Resistance Variation with Gate to Source Voltage

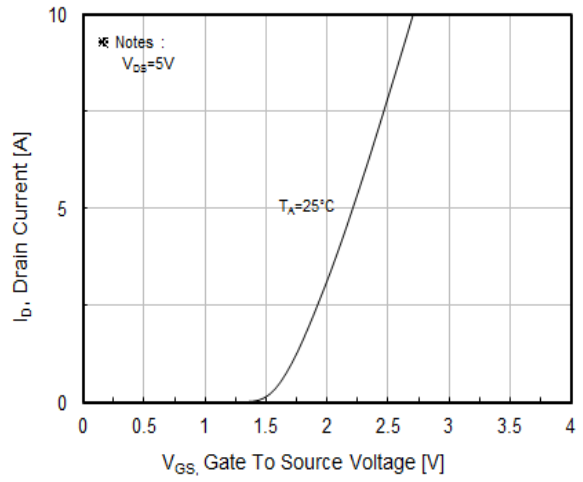


Fig.5 Transfer Characteristics

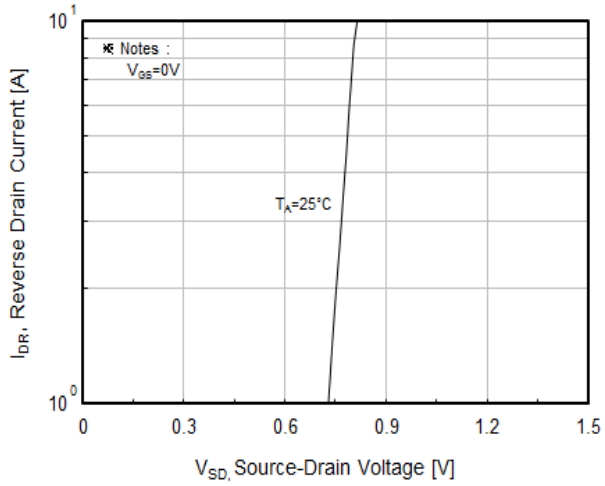


Fig.6 Body Diode Forward Voltage Variation with Source Current

Characteristic Graph

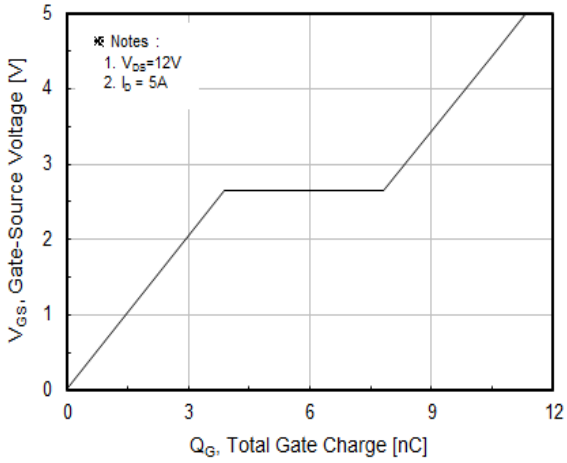


Fig.7 Gate Charge Characteristics

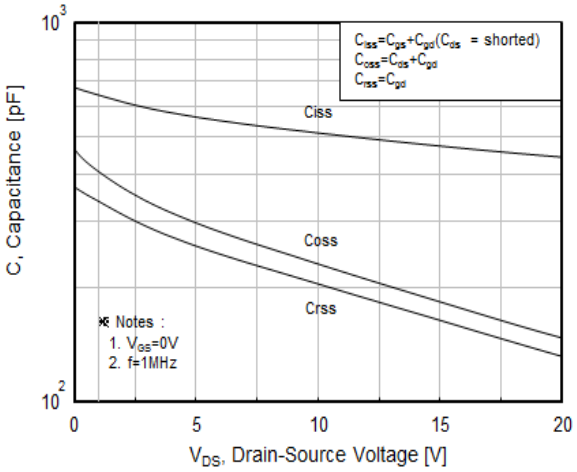


Fig.8 Capacitance Characteristics

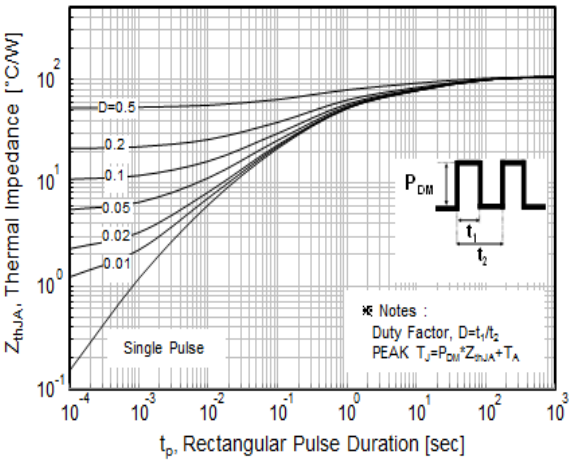


Fig.9 Transient Thermal Impedance Curve

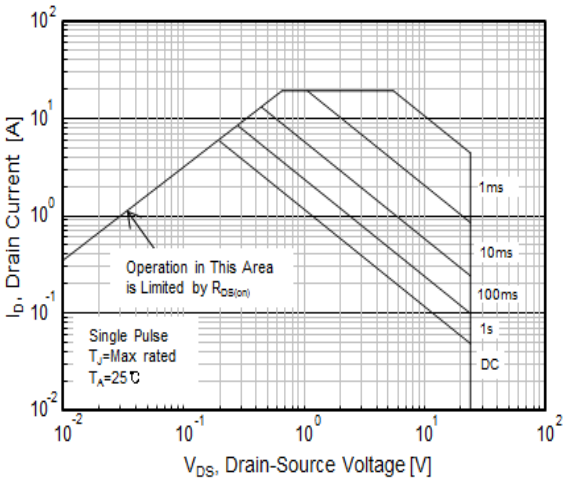
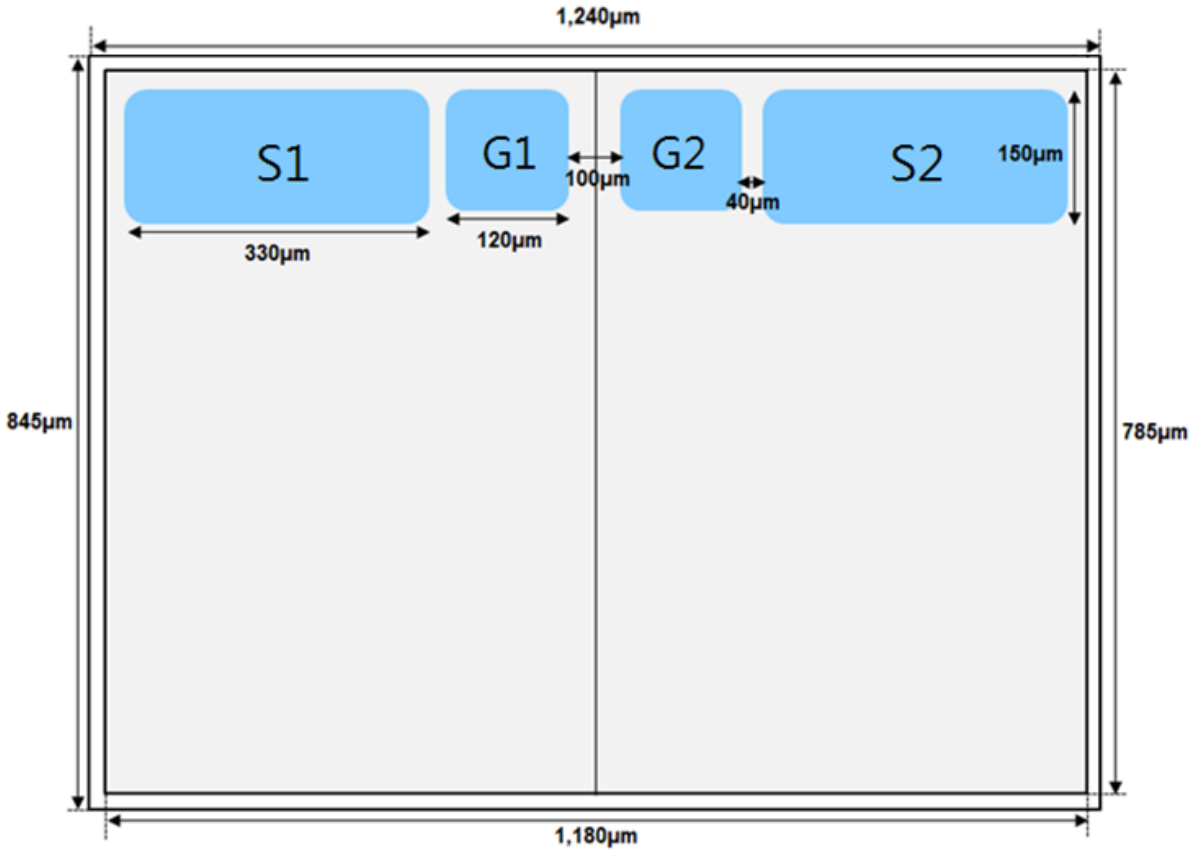


Fig.10 Maximum Safe Operating Area

Die Outline (Unit : um)



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