MDW0301E

Common-Drain Dual N-Channel Trench MOSFET 24V

General Description

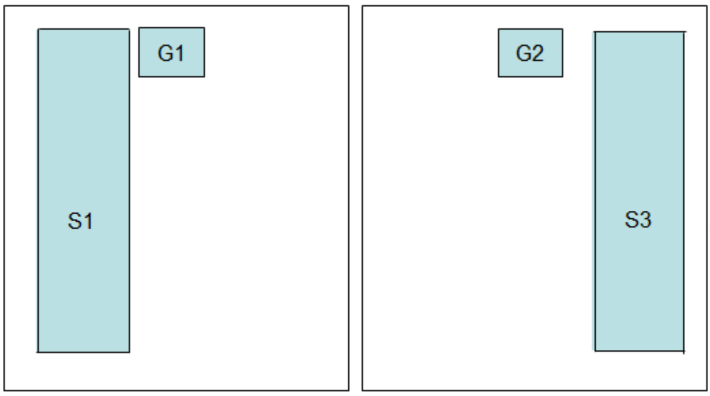
The MDW0301E uses advanced MagnaChip's MOSFET Technology, which provides high performance in on-state resistance, fast switching performance and excellent quality. Excellent low $R_{DS(ON)}$, low gate charge and operation for Battery Application.

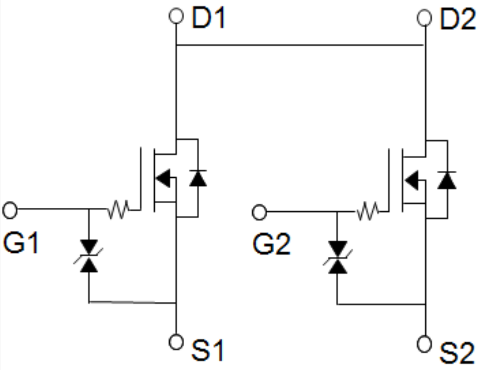
Features

- V_{DS} = 24V
- Drain-Source ON Resistance;
  - $R_{DS(ON)}$ < 8.0mΩ @ V_{GS} = 3.0V
  - $R_{DS(ON)}$ < 6.4mΩ @ V_{GS} = 3.9V

Applications

- Portable Battery Protection Module





Chip Layout
(Drain is the backside of the wafer (TOP View))

Absolute Maximum Ratings (Ta = 25°C unless otherwise noted) Note 1

Characteristics	*Symbol*	*Rating*	*Units*
Drain-Source Voltage	V_{DSS}	*24*	*V*
Gate-Source Voltage	V_{GSS}	*±12*	*V*
Junction and Storage Temperature Range	T_J, T_{stg}	*-55~150*	*°C*

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Electrical Characteristics (Ta =25^{o}C unless otherwise noted)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	24	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.5	1.0	1.5	
Drain Cut-Off Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V	-	-	1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0V	-	-	10.0	μA
Drain-Source Resistance Note 2	$R_{DS(ON)}$	V_{GS} = 3.0V, I_D = 3.0A	-	6.4	8.0	mΩ
		V_{GS} = 3.9V, I_D = 3.0A	-	5.4	6.4	
Forward Transconductance	g_{fs}	V_{DS} = 5V, I_D = 8.0A	-	40	-	S
Dynamic Characteristics Note 3						
Total Gate Charge	Q_g	V_{DS} = 12V, I_D = 8.0A, V_{GS} = 4.5V	-	21	-	nC
Gate-Source Charge	Q_{gs}		-	5.8	-	
Gate-Drain Charge	Q_{gd}		-	9.6	-	
Input Capacitance	C_{iss}	V_{DS} = 12V, V_{GS} = 0V, f = 1MHz	-	1770	-	pF
Reverse Transfer Capacitance	C_{rss}		-	394	-	
Output Capacitance	C_{oss}		-	453	-	
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 5.0V, V_{DS} = 15V, I_D = 8A, R_G = 6 Ω	-	18	-	us
Rise Time	t_r		-	19.5	-	
Turn-Off Delay Time	$t_{d(off)}$		-	1.6	-	
Fall Time	t_f		-	0.8	-	
Drain-Source Body Diode Characteristics Note 3						
Source-Drain Diode Forward Voltage	V_{SD}	I_S = 1.0A, V_{GS} = 0V	-	0.65	1	V

Notes :

1. The device current rating is derived from its thermal resistance and from the number and diameter of bonding wires. The testing current at wafer level is set only for ease of testing. Actual package current ratings can be much higher.

2. $R_{DS(ON)}$ is Single MOS . In this case, $R_{DS(ON)}$ is $R_{SS(ON)}$ / 2

3. Dynamic Characteristics and Drain-Source Body Diode Characteristics are tested on TSSOP-8 Package.

4. No SOA curves are provided because they are dependent on package thermal resistance

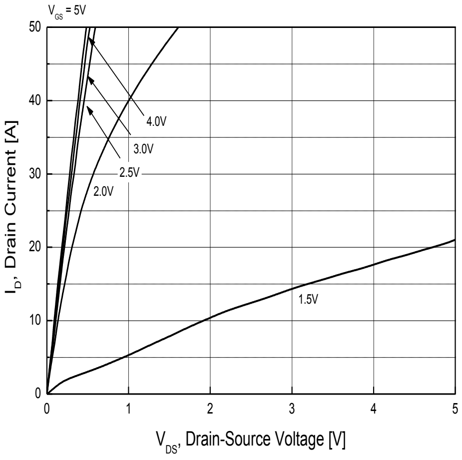


Fig.1 On-Region Characteristics

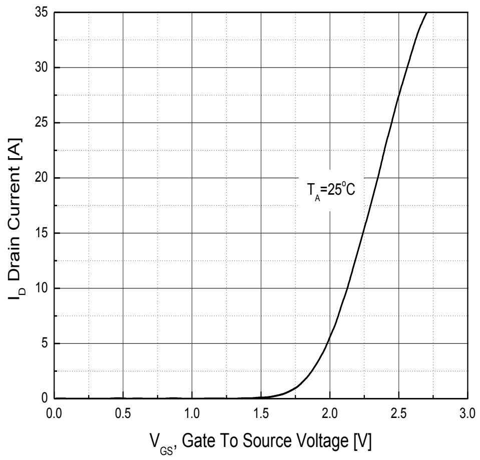


Fig.2 Transfer Characteristics

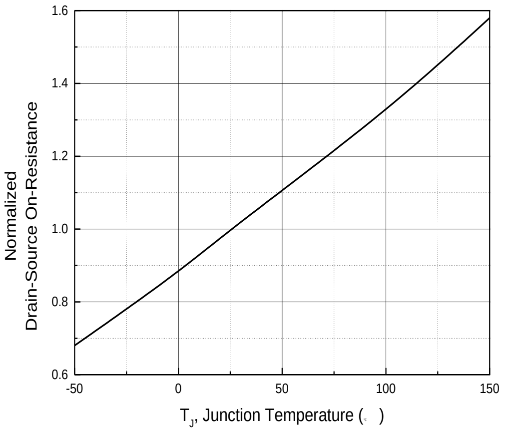


Fig.3 On-Resistance Variation with Temperature

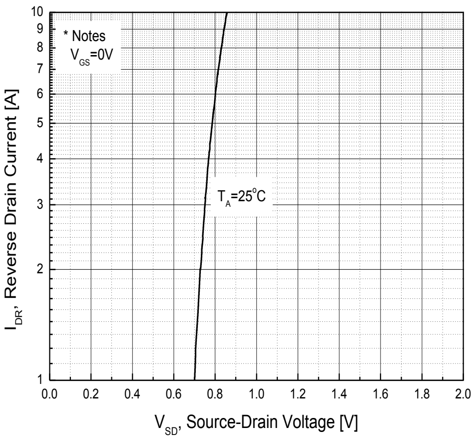


Fig.4 Body Diode Forward Voltage Variation with Source Current and Temperature

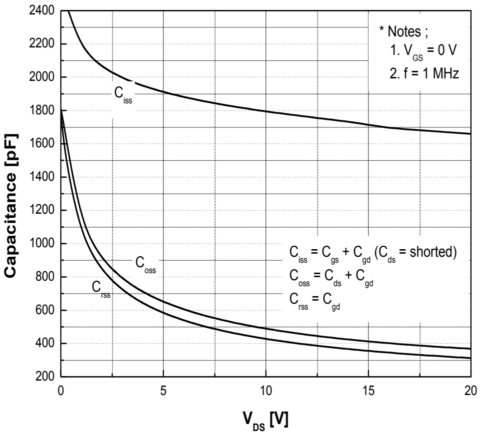
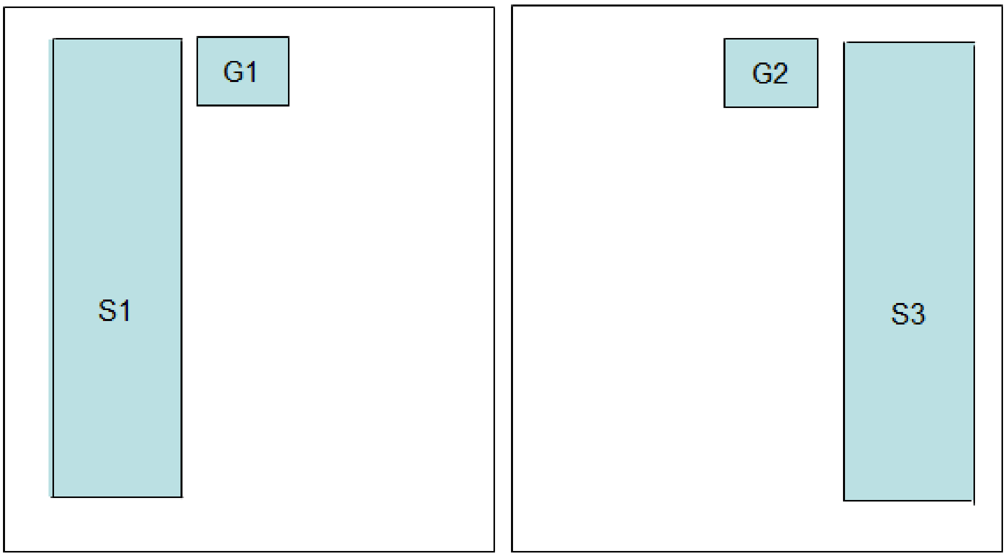


Fig.5 Capacitance Characteristics

Die Layout and Construction



Contents	Value
Wafer Thickness	158±10 ㎛
Metal (Top)	Al-Cu-Si
Metal (Back)	V/Ni/Ag
Passivation Layer	Yes
Die Size (With Scribe lane)	2,630×1,300 ㎛ ^{2}
Scribe lane width	60 ㎛
Gate Pad Open Size	160 ×200 ㎛ ^{2}
Gross Die (per Wafer)	8,138ea

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