



AMDU040N008PSVRH

Single N-channel Trench MOSFET 40V 0.8mΩ

FEATURES

- Trench power MOSFET technology
- Single N-channel trench, normal gate level
- Enhanced avalanche ruggedness
- 100% Avalanche tested
- Maximum 175°C junction temperature

PRODUCT VALIDATION

- Qualified according to AEC-Q101 Standard

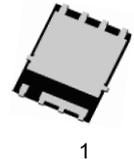
KEY PERFORMANCE PARAMETERS

V_{DS}	40	V
$R_{DS(on), typ.}$	0.00066	Ω
I_D	371	A
Q_g	95	nC
Junction temperature, $_{max}$	175	$^{\circ}C$

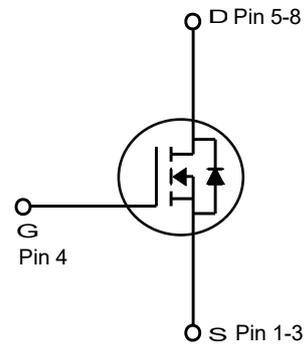


Top View

PDFN56



Bottom View



ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
AMDU040N008PSVRH	PDFN56	040N008P	Tape & Reel	Halogen Free

<http://www.magnachip.com>

ABSOLUTE MAXIMUM RATINGS, at $T_C = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Rating	Unit
Drain-source Voltage	V_{DS}	40	V
Gate-source Voltage	V_{GS}	± 20	
Drain current	I_D	$T_C=25^\circ\text{C}$ (Silicon Limited)	371
		$T_C=25^\circ\text{C}$ (Package Limited)	190
		$T_C=100^\circ\text{C}$ (Silicon Limited)	263
¹⁾ Pulsed drain current	I_{DM}	$T_C=25^\circ\text{C}$, $t_p \leq 100\mu\text{s}$	1349
Total power dissipation	P_{tot}	$T_C=25^\circ\text{C}$	188
		$T_C=100^\circ\text{C}$	94
²⁾ Avalanche energy, single pulse	E_{AS}		450
Operating and storage temperature	T_j, T_{stg}	- 55 ~ 175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Parameter	Symbol	Rating	Unit
Thermal resistance, junction - case	$R_{\theta JC}$	0.8	$^\circ\text{C/W}$
³⁾ Thermal resistance, junction - ambient	$R_{\theta JA}$	50	

ELECTRICAL CHARACTERISTICS (T_j = 25°C)**STATIC CHARACTERISTICS**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Drain-source breakdown voltage	V _{(BR)DSS}	40	-	-	V	V _{GS} =0 V, I _D =250 μA
Gate threshold voltage	V _{GS(th)}	2.25	-	3.75	V	V _{DS} =V _{GS} , I _D =552 μA
Zero gate voltage drain current	I _{DSS}	-	-	1	μA	V _{DS} =40 V, V _{GS} =0 V
Gate-source leakage current	I _{GSS}	-	-	± 100	nA	V _{GS} =±20 V, V _{DS} =0 V
Drain-source on-state resistance	R _{DS(on)}	-	0.66	0.80	mΩ	V _{GS} =10 V, I _D =50 A
		-	0.80	1.10		V _{GS} =8 V, I _D =50 A
⁴⁾ Gate resistance	R _g	-	1.0	-	Ω	f=1 MHz
⁴⁾ Transconductance	g _{fs}	-	97	-	S	V _{DS} =10 V, I _D =50 A

⁴⁾ DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Input capacitance	C _{iss}	-	6908	-	pF	V _{GS} =0 V, V _{DS} =20 V, f=1 MHz
Output capacitance	C _{oss}	-	1996	-		
Reverse transfer capacitance	C _{rss}	-	64	-		
Turn-on delay time	t _{d(on)}	-	32	-	ns	V _{DD} =20 V, V _{GS} =10 V, I _D =50 A, R _{G,ext} =1.6 Ω
Rise time	t _r	-	16	-		
Turn-off delay time	t _{d(off)}	-	55	-		
Fall time	t _f	-	17	-		

⁴⁾ GATE CHARGE CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Gate to source charge	Q _{gs}	-	28	-	nC	V _{DD} =32 V, I _D =50 A, V _{GS} =0 to 10 V
Gate charge at threshold	Q _{gs(th)}	-	9	-		
Gate to drain charge	Q _{gd}	-	20	-		
Switching charge	Q _{sw}	-	29	-		
Gate charge total	Q _g	-	95	-		
Gate plateau voltage	V _{plateau}	-	5.2	-	V	

SOURCE-DRAIN DIODE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
⁴⁾ Diode continuous forward current	I _S	-	-	190	A	-
⁴⁾ Diode pulse current	I _{S,pulse}	-	-	1349		pulsed; t _p ≤ 100 μs
Diode forward voltage	V _{SD}	-	0.78	1.0	V	V _{GS} =0 V, I _F =50 A
⁴⁾ Reverse recovery time	t _{rr}	-	59	-	ns	I _F =50 A, di _F /dt=100 A/μs
⁴⁾ Reverse recovery charge	Q _{rr}	-	64	-	nC	

Notes

- Pulse width limited by T_{jmax}
- Starting T_j=25°C, L=1mH, I_{AS}=30A, V_{DD}=36V, V_{GS}=10V
- Surface mounted FR-4 board by JEDEC (jesd51-7)
- The parameter is not subject to production testing - guaranteed by design.

ELECTRICAL CHARACTERISTICS DIAGRAMS

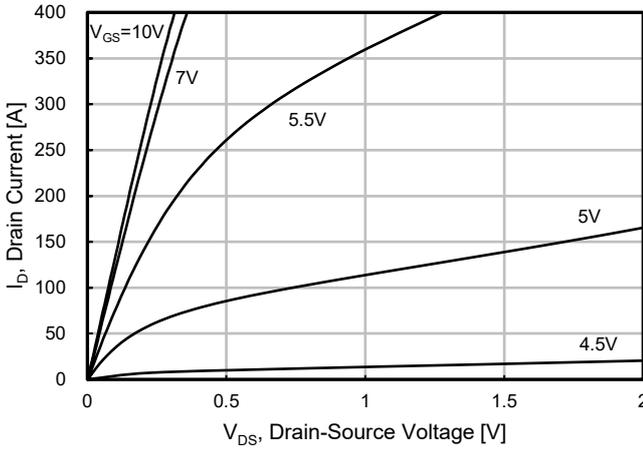


Fig. 1. Typ. Output Characteristics

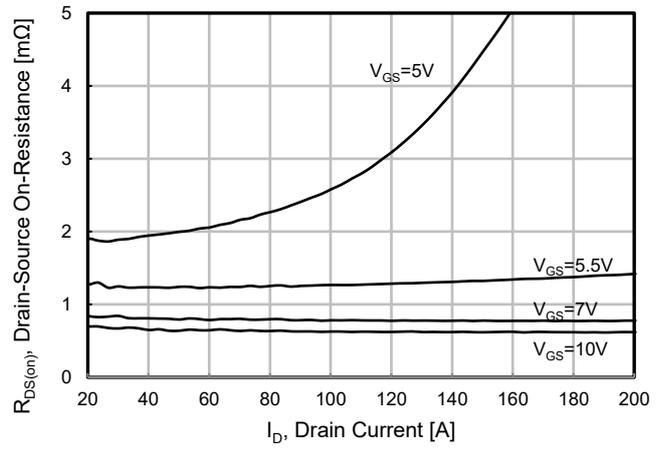


Fig. 2. Typ. Drain-Source On-Resistance

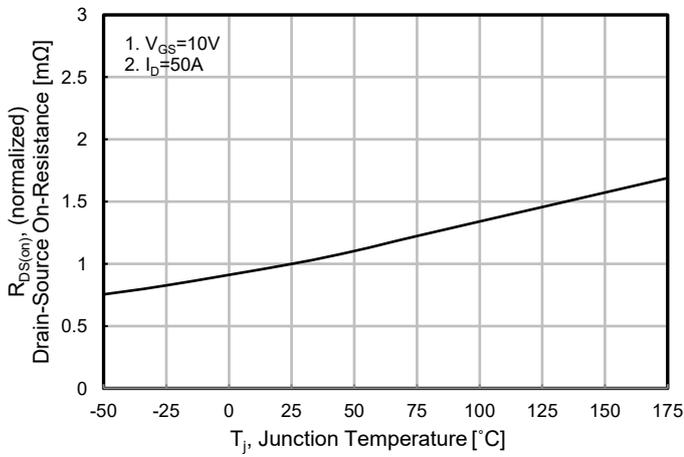


Fig. 3. On-Resistance vs. Junction Temperature

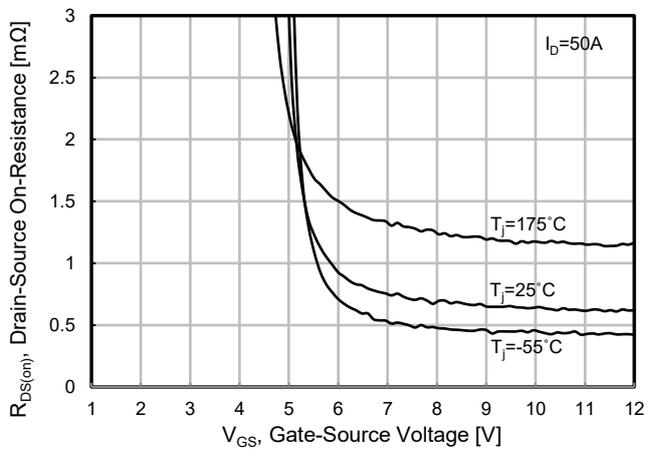


Fig. 4. On-Resistance vs. Gate-Source Voltage

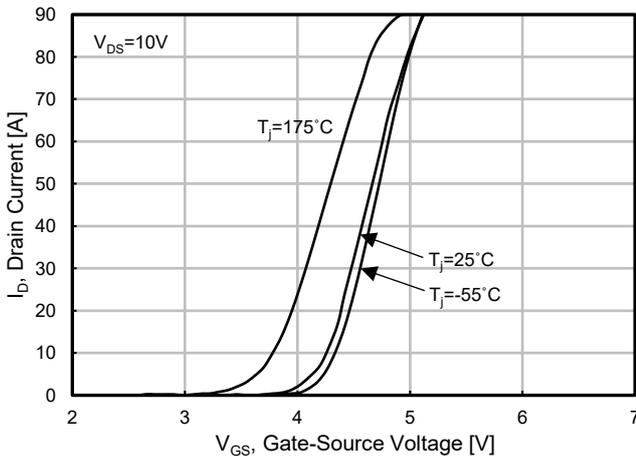


Fig. 5. Transfer Characteristics

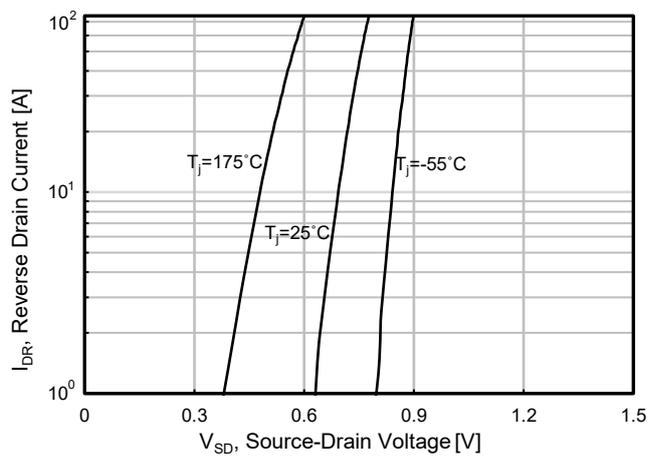


Fig. 6. Forward Characteristics of Reverse Diode

ELECTRICAL CHARACTERISTICS DIAGRAMS

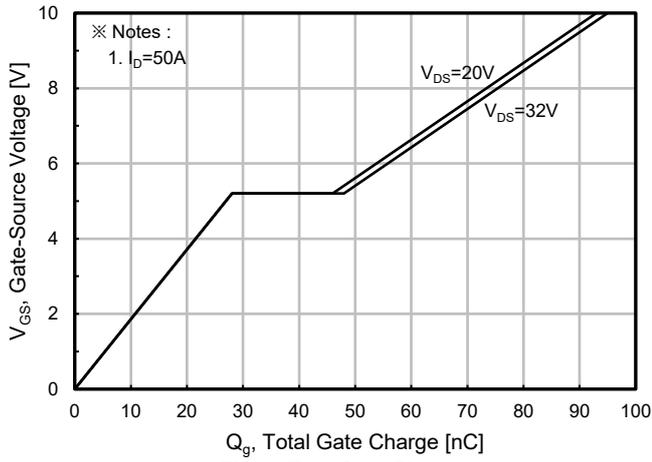


Fig. 7. Typ. Gate Charge

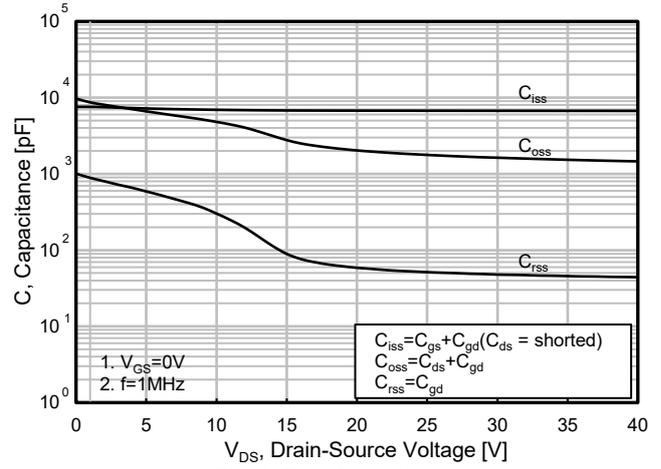


Fig. 8. Typ. Capacitance

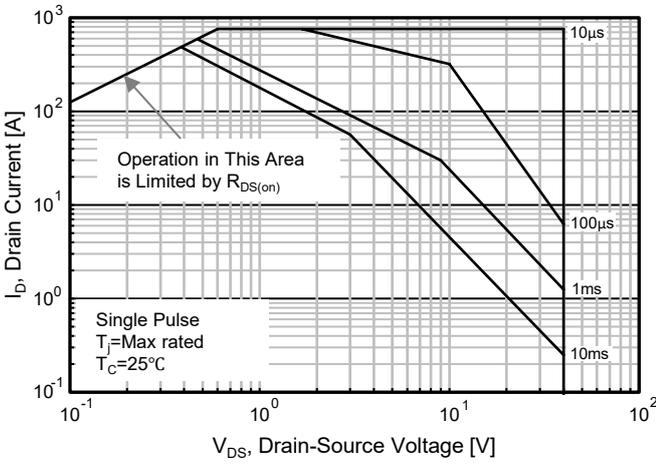


Fig. 9. Safe Operating Area

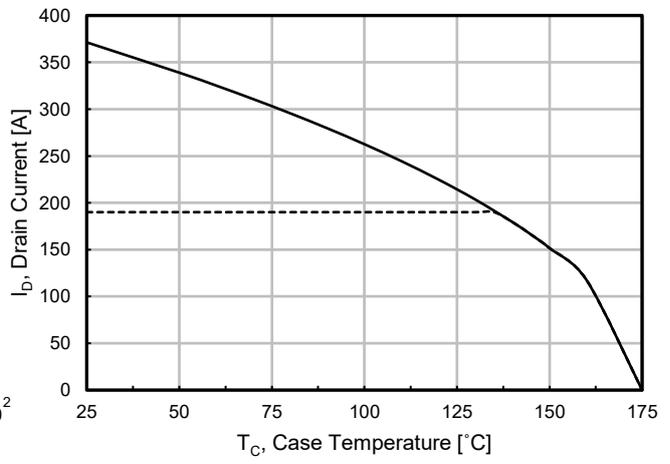


Fig. 10. Drain Current vs. Temperature

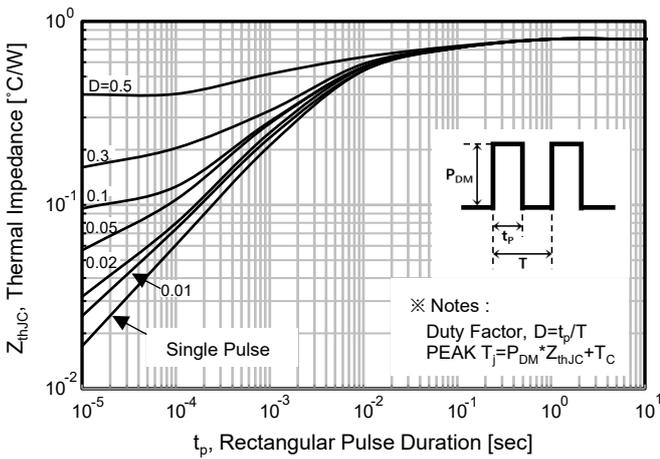


Fig. 11. Transient Thermal Impedance

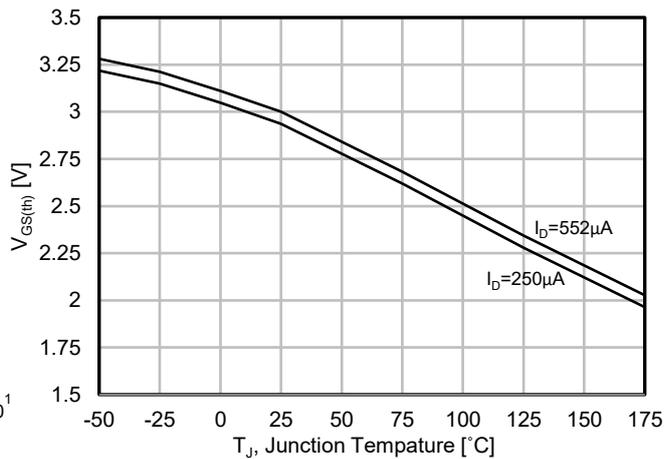


Fig. 12. V_GS(th) Variation with Temperature

ELECTRICAL CHARACTERISTICS DIAGRAMS

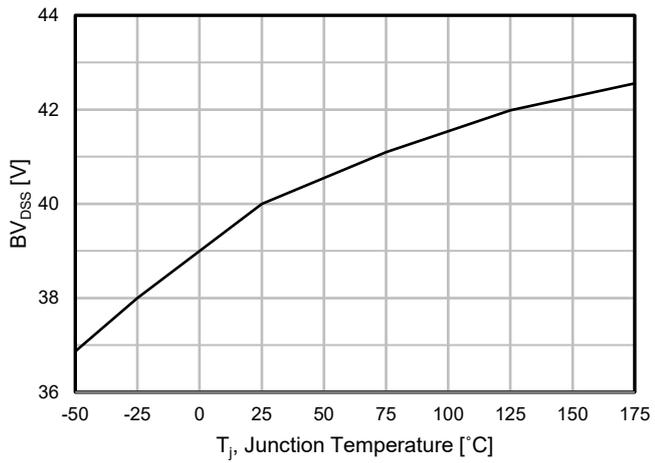
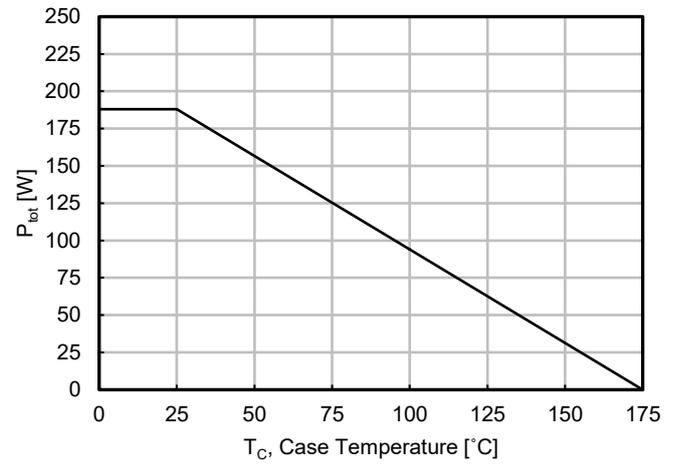
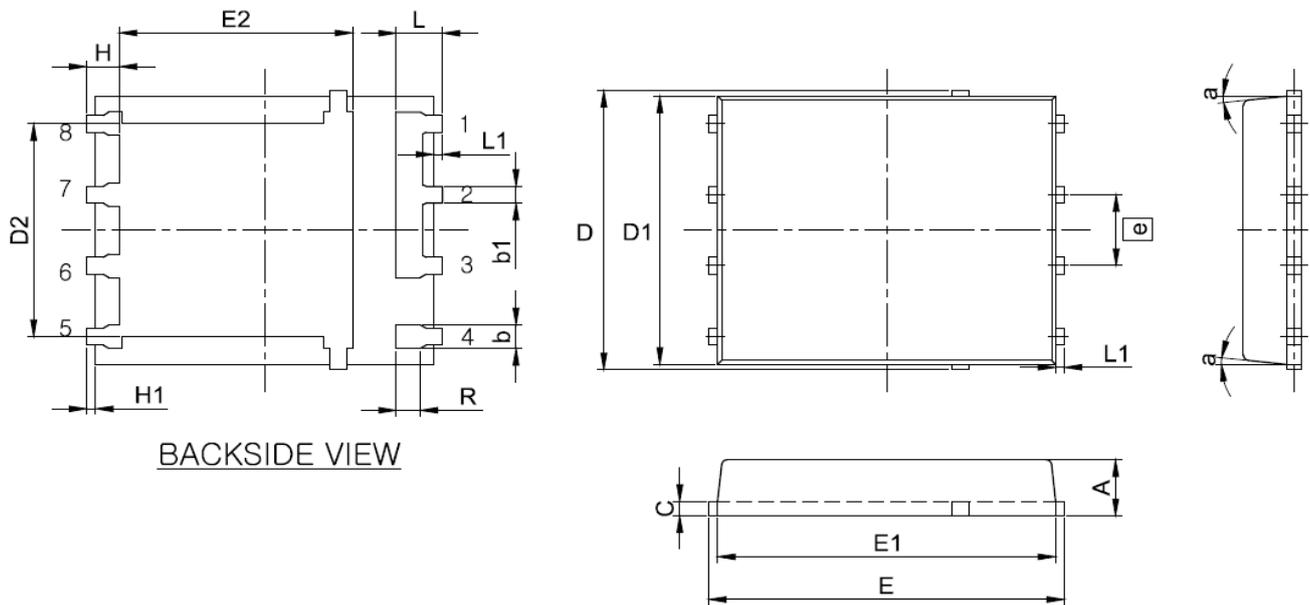
Fig. 13. BV_{DSS} Variation with Temperature

Fig. 14. Power Dissipation

Package Outlines

PDFN56



Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.90	-	1.10
b	0.33	-	0.49
b1	0.26	-	1.36
C	0.20	0.25	0.34
D	4.50	5.15	5.30
D1	4.50	5.00	5.10
D2	3.65	-	3.95
E	5.90	6.15	6.30
E1	5.85	6.00	6.10
E2	3.46	-	3.86
e	1.27 BSC		
H	0.50	-	0.71
H1	0.03	-	0.13
L	0.74	-	0.84
L1	0.03	-	0.13
R	0.48	-	0.58
a	0°	-	12°

Notes

Package body size, length and width do not include mold flash, protrusions and gate burrs.

DISCLAIMER :

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

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