

MMSFA60R115S6Z

600V 0.115Ω N-channel MOSFET

Description

Superior 6th generation SJ MOSFETs (S6-series) are cutting-edge high voltage power MOSFETs, based on Magnachip's extensive design expertise and years of experience. The main strengths of S6-series are low on-resistance, low gate charge and reduced tendency for ringing. As a result, its switching loss is very low, making it optimized for switching applications. Moreover, these user-friendly devices offer the advantages of improved ruggedness and remarkable ESD capability by integrated Zener diode, making it an ideal choice for designers.

Key Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	0.115	Ω
$V_{TH,typ}$	3.5	V
I_D	26	A
$Q_{g,typ}$	43.9	nC

Features

- Low power loss by high speed switching and low on-resistance
- 100% avalanche tested
- Green package – Pb free plating, Halogen free
- Zener-integrated

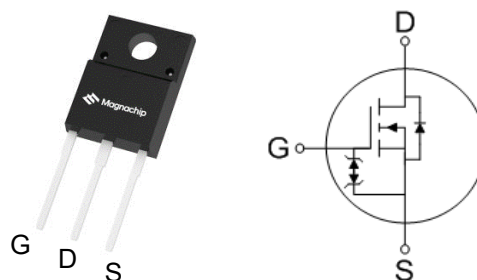
Applications

- PFC power supply stages
- Switching applications
- Adapters
- DC-DC converters

Ordering Information

Order Code	Marking	Temp. ange	Package	Packing	RoHS Status
MMSFA60R115S6ZTH	A60R115S6ZS	-55 ~ 150°C	TO-220SFA	Tube	Compliant

Package & internal circuit



■ Absolute Maximum Rating ($T_c=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit	Note
Drain – source voltage	V_{DSS}	600	V	
Gate – source voltage	V_{GSS}	± 25	V	
Continuous drain current ¹⁾	I_{D}	26	A	$T_c=25^{\circ}\text{C}$
		16.4	A	$T_c=100^{\circ}\text{C}$
Pulsed drain current ²⁾	I_{DM}	78	A	
Power dissipation	P_{D}	28	W	
Single - pulse avalanche energy ³⁾	E_{AS}	82	mJ	
MOSFET dv/dt ruggedness	dv/dt	80	V/ns	
Continuous diode forward current	I_{SD}	26	A	
Diode dv/dt ruggedness ⁴⁾	dv/dt	50	V/ns	
Storage temperature	T_{stg}	-55 ~150	$^{\circ}\text{C}$	
Maximum operating junction temperature	T_{j}	150	$^{\circ}\text{C}$	

1) I_{D} limited by maximum junction temperature, Duty cycle $D=0.5$

2) Pulse width t_{p} limited by $T_{\text{j,max}}$

3) $I_{\text{AS}} : 3.7 \text{ A}$

4) $I_{\text{SD}} \leq I_{\text{D}}$, $V_{\text{DS peak}} \leq 400\text{V}$, $di/dt \leq 900\text{A}/\mu\text{s}$

■ Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case max	R_{thJC}	4.46	$^{\circ}\text{C}/\text{W}$
Thermal resistance, junction-ambient max	R_{thJA}	65.3	$^{\circ}\text{C}/\text{W}$

■ Static Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain – source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS} = 0V, I_D = 1mA$
Gate Threshold Voltage	$V_{GS(th)}$	2.5	3.5	4.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS} = 600V, V_{GS} = 0V$
Gate leakage current	I_{GSS}	-	-	10	μA	$V_{GS} = \pm 25V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(ON)}$	-	0.103	0.115	Ω	$V_{GS} = 10V, I_D = 8.2A$

■ Dynamic Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input capacitance	C_{iss}	-	1933	-	pF	$V_{DS} = 400V, V_{GS} = 0V, f = 250kHz$
Output capacitance	C_{oss}	-	41	-		
Reverse transfer capacitance	C_{rss}	-	4.7	-		
Effective output capacitance energy related ⁵⁾	$C_{o(er)}$	-	58	-		$V_{DS} = 0V \text{ to } 400V, V_{GS} = 0V, f = 250kHz$
Effective output capacitance time related ⁶⁾	$C_{o(tr)}$		346			$V_{DS} = 0V \text{ to } 400V, V_{GS} = 0V, f = 250kHz$
Turn on delay time	$t_{d(on)}$	-	37	-	ns	$V_{GS} = 10V, R_G = 25\Omega, V_{DD} = 300V, I_D = 26A$
Rise time	t_r	-	53	-		
Turn off delay time	$t_{d(off)}$	-	91	-		
Fall time	t_f	-	24	-		
Total gate charge	Q_g	-	37	-	nC	$V_{GS} = 10V, V_{DD} = 400V, I_D = 8.2A$
Gate – source charge	Q_{gs}	-	9.6	-		
Gate – drain charge	Q_{gd}	-	14.6	-		
Gate resistance	R_G	-	3.5	-	Ω	$V_{GS} = 0V, f = 1MHz$

5) $C_{o(er)}$ is a capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

6) $C_{o(tr)}$ is a capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

■ Reverse Diode Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Diode forward voltage	V_{SD}	-	-	1.4	V	$I_{SD} = 8.2\text{A}$, $V_{GS} = 0\text{V}$
Reverse recovery time	t_{rr}	-	249	-	ns	$I_{SD} = 8.2\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 400\text{V}$
Reverse recovery charge	Q_{rr}	-	2.4	-	μC	
Reverse recovery current	I_{rrm}	-	19	-	A	

■ Characteristic graph

Fig.1 On-region characteristics.

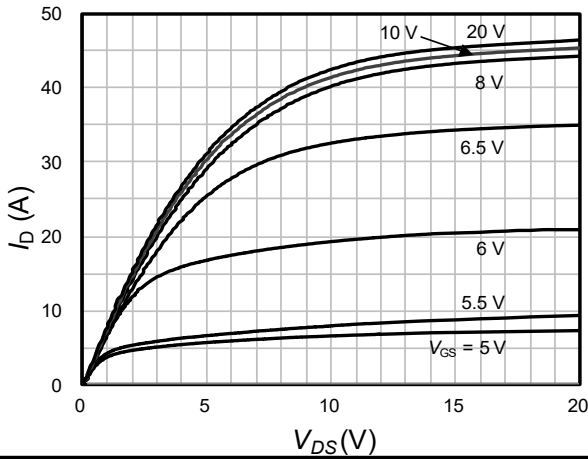


Fig.2 On-resistance variation with drain current

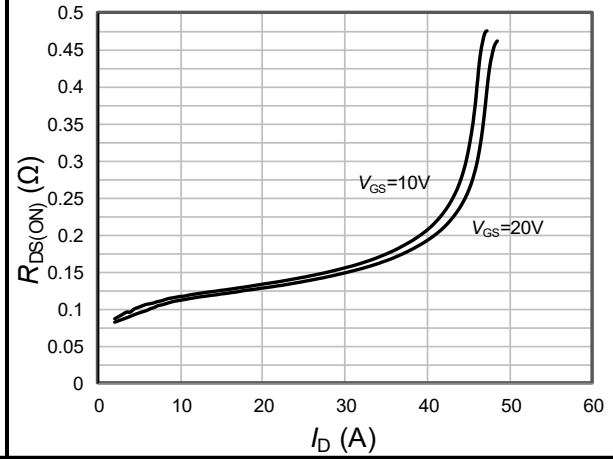


Fig.3 On-resistance variation with junction temperature (normalized)

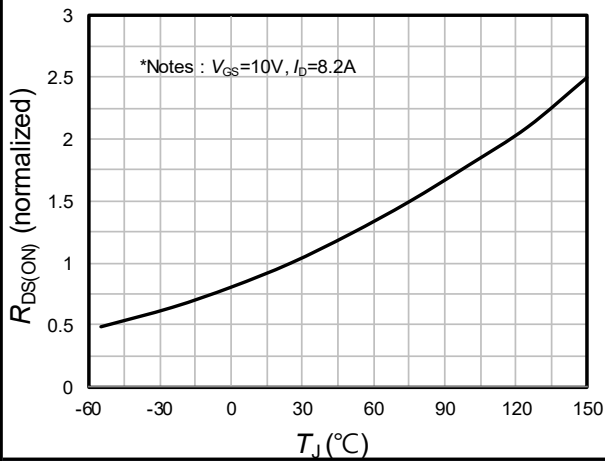


Fig.4 Breakdown voltage variation with temperature (normalized)

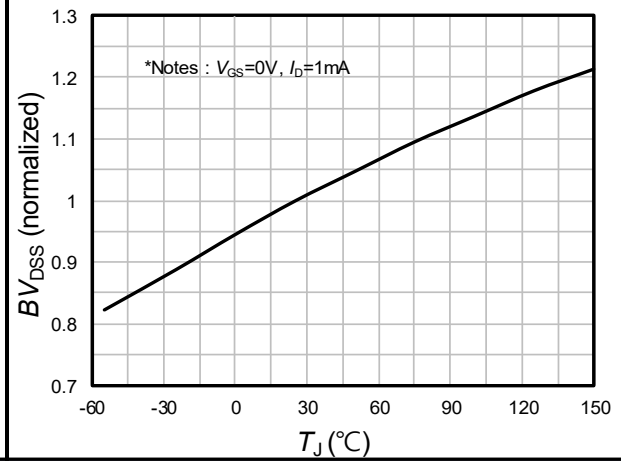


Fig.5 Transfer characteristics

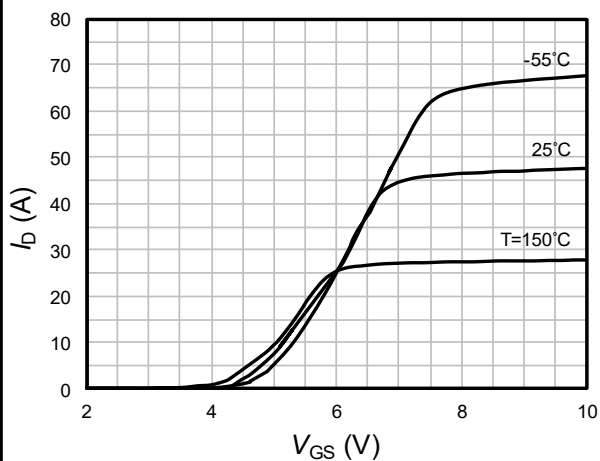


Fig.6 Diode forward characteristics

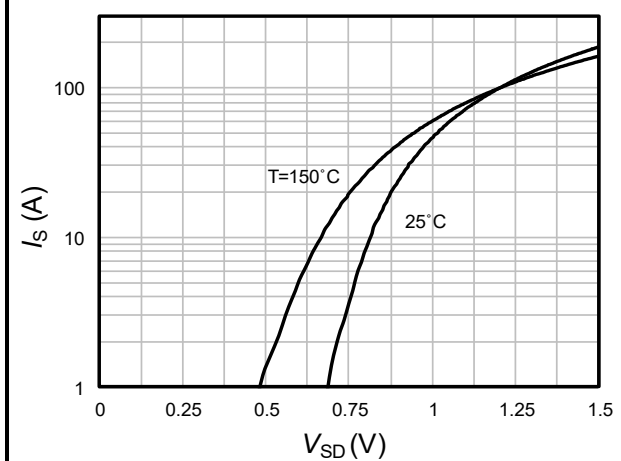


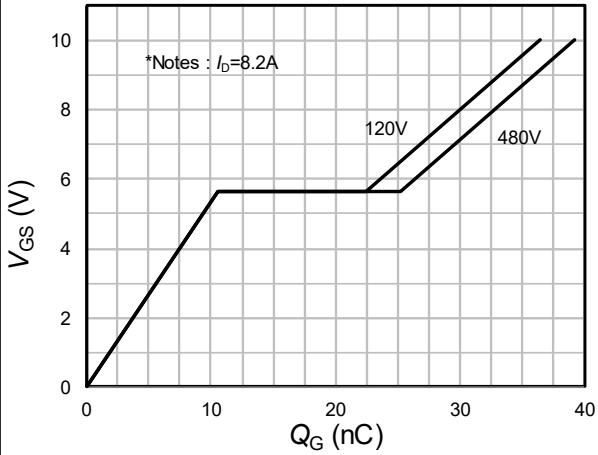
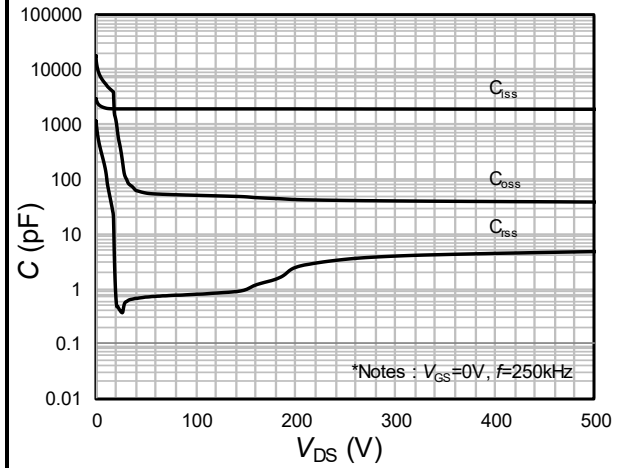
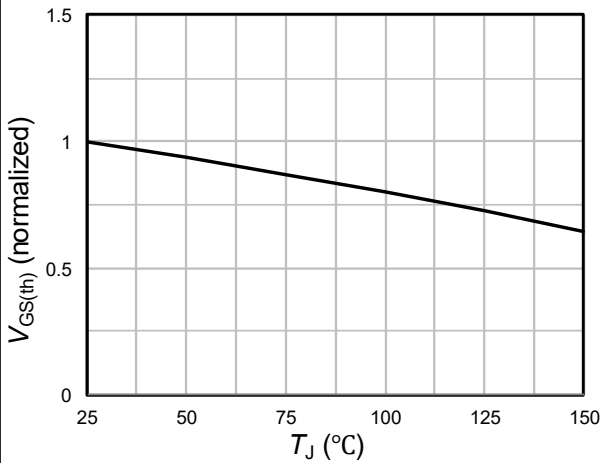
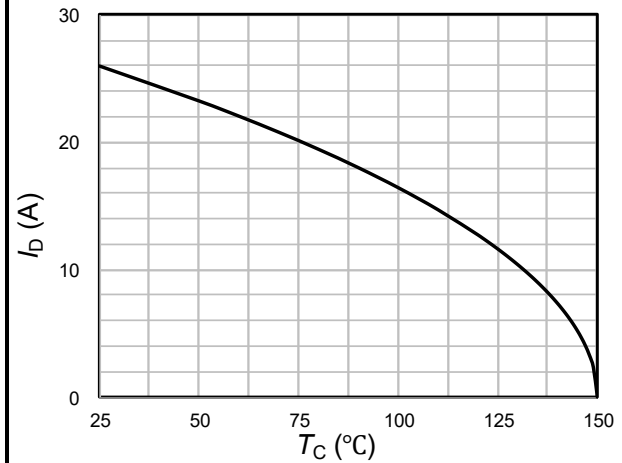
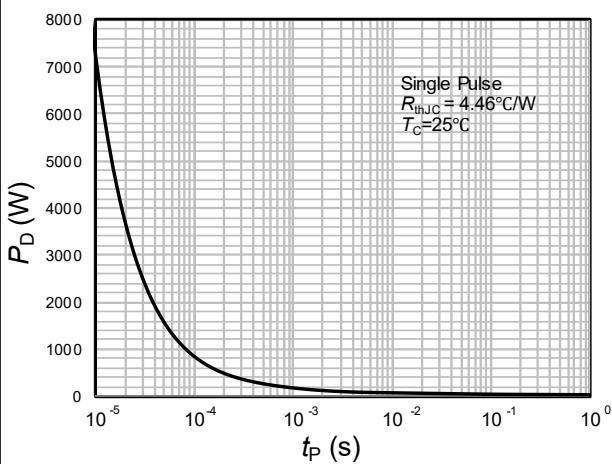
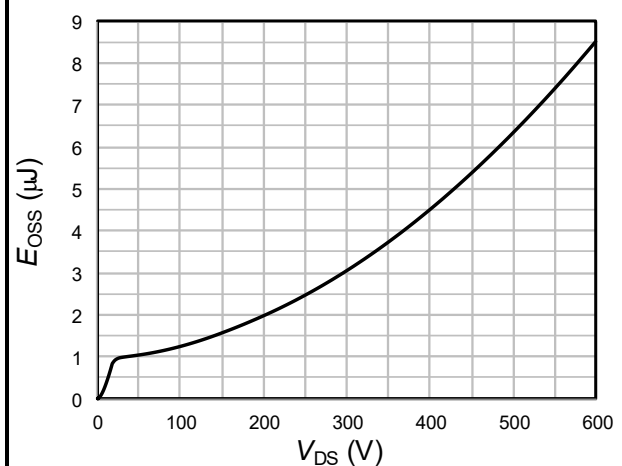
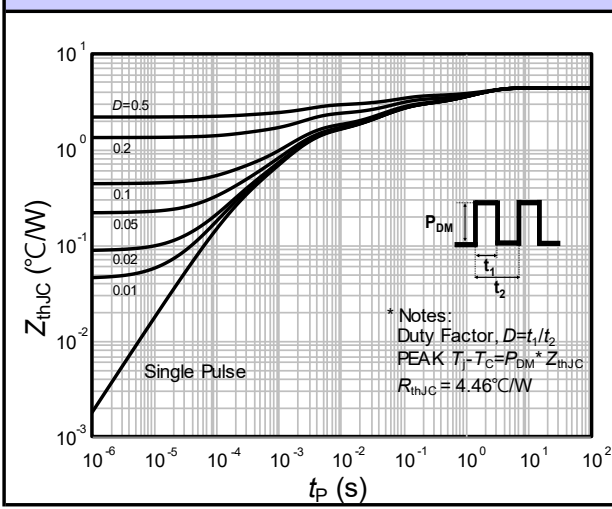
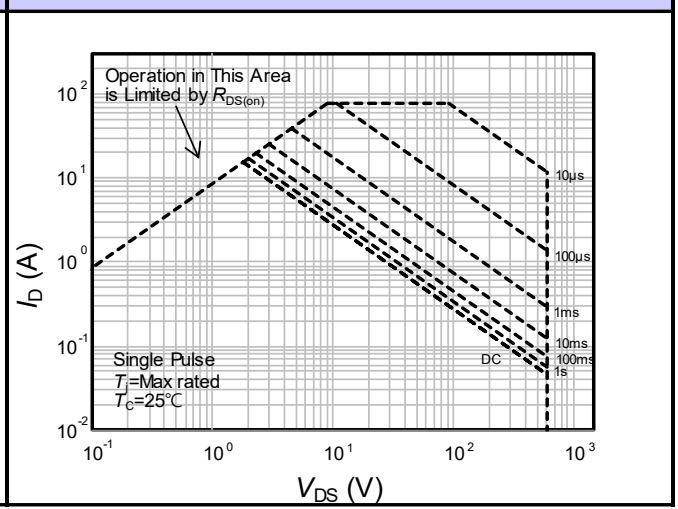
Fig.7 Gate charge characteristics

Fig.8 Capacitance characteristics

Fig.9 Threshold voltage variation with junction temperature

Fig.10 Drain current

Fig.11 Power dissipation variation with pulse time

Fig.12 Output capacitance stored energy


Fig.13 Transient thermal response

Fig.14 Safe operating area


The graph shows the relationship between gate voltage (V_{GS}) and charge. The curve starts at the origin, rises linearly through the accumulation region (labeled Q_g), then levels off through the depletion region (labeled $Q_{gs} + Q_{gd}$), and finally rises linearly again in the inversion region. The depletion region is further divided into Q_{gs} (charge on the gate) and Q_{gd} (charge in the depletion region). A dashed line indicates a constant voltage level of 10V.

DISCLAIMER:

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