MDU040N007PSLVRH

Single N-channel Trench MOSFET 40V 0.7mΩ

FEATURES

- **Trench power MOSFET technology**
- **Single N-channel trench, logic gate level**
- **Enhanced avalanche ruggedness**
- **100% Avalanche tested**
- **Maximum 175°C junction temperature**

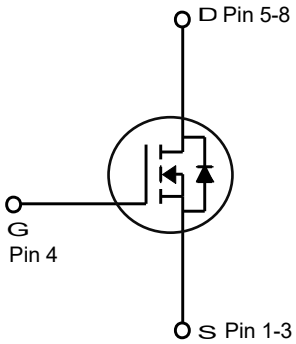
Top View

PDFN56

Bottom View

PRODUCT VALIDATION

- **Qualified according to JEDEC Standard**



KEY PERFORMANCE PARAMETERS

V_{DS}	**40**	V
$R_{DS(on),\ typ.}$	**0.00058**	Ω
I_D	**397**	A
Q_g	**109**	nC
Junction temperature, max	**175**	°C

RoHS Compliant
HALOGEN-FREE

ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
MDU040N007PSLVRH	PDFN56	040N007PL	Tape & Reel	Halogen Free

http://www.magnachip.com

ABSOLUTE MAXIMUM RATINGS, at T_C = 25℃, unless otherwise specified

Parameter		Symbol	Rating	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 18	
Drain current	Tc=25°C	I_D	397	A
	Tc=100°C		281	
[1] Pulsed drain current	Tc=25°C	I_{DM}	1588	
Total power dissipation	Tc=25°C	P_{tot}	188	W
	Tc=100°C		94	
[2] Avalanche energy, single pulse		E_{AS}	450	mJ
Operating and storage temperature		T_j, T_{stg}	- 55 ~ 175	°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Rating	Unit
Thermal resistance, junction - case	$R_{\theta JC}$	0.8	°C/W
[3] Thermal resistance, junction - ambient	$R_{\theta JA}$	50	

ELECTRICAL CHARACTERISTICS (T_j = 25°C)

STATIC CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=250 μA
Gate threshold voltage	$V_{GS(th)}$	1.30	1.80	2.30		V_{DS}=V_{GS}, I_D=552 μA
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=40 V, V_{GS}=0 V
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	V_{GS}=±18 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.58	0.70	mΩ	V_{GS}=10 V, I_D=50 A
		-	0.84	1.20		V_{GS}=4.5 V, I_D=50 A
[4] Gate resistance	R_g	-	1.0	-	Ω	f=1 MHz
[4] Transconductance	g_{fs}	-	160	-	S	V_{DS}=10 V, I_D=50 A

[4] DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Input capacitance	C_{iss}	-	7104	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance	C_{oss}	-	1855	-		
Reverse transfer capacitance	C_{rss}	-	61	-		
Turn-on delay time	$t_{d(on)}$	-	26	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	6	-		
Turn-off delay time	$t_{d(off)}$	-	65	-		
Fall time	t_f	-	15	-		

[4] GATE CHARGE CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Gate to source charge	Q_{gs}	-	20	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{gs(th)}$	-	8	-		
Gate to drain charge	Q_{gd}	-	15	-		
Switching charge	Q_{sw}	-	27	-		
Gate charge total	Q_g	-	109	-		
Gate plateau voltage	$V_{plateau}$	-	3.4	-	V	

SOURCE-DRAIN DIODE

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
[4] Diode continuous forward current	I_S	-	-	190	A	-
[4] Diode pulse current	$I_{S,pulse}$	-	-	1449		pulsed; $t_p \leq$ 100 μs
Diode forward voltage	V_{SD}	-	0.78	1.0	V	V_{GS}=0 V, I_F=50 A
[4] Reverse recovery time	t_{rr}	-	57	-	ns	I_F=50 A, di_F/dt=100 A/μs
[4] Reverse recovery charge	Q_{rr}	-	77	-	nC	

Notes
1. Pulse width limited by T_{jmax}
2. Starting T_j=25°C, L=1mH, I_{AS}=30A, V_{DD}=36V, V_{GS}=10V
3. Surface mounted FR-4 board by JEDEC (jesd51-7)
4. The parameter is not subject to production testing - guaranteed by design.

ELECTRICAL CHARACTERISTICS DIAGRAMS

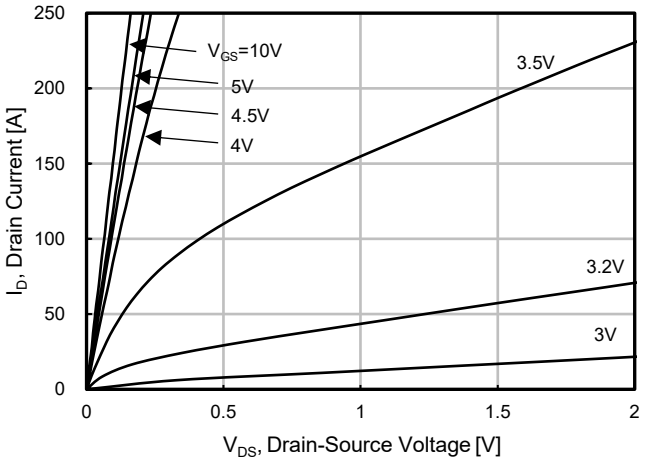


Fig. 1. Typ. Output Characteristics

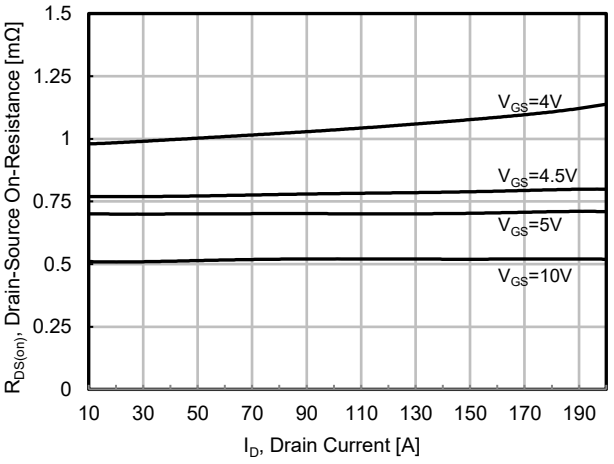


Fig. 2. Typ. Drain-Source On-Resistance

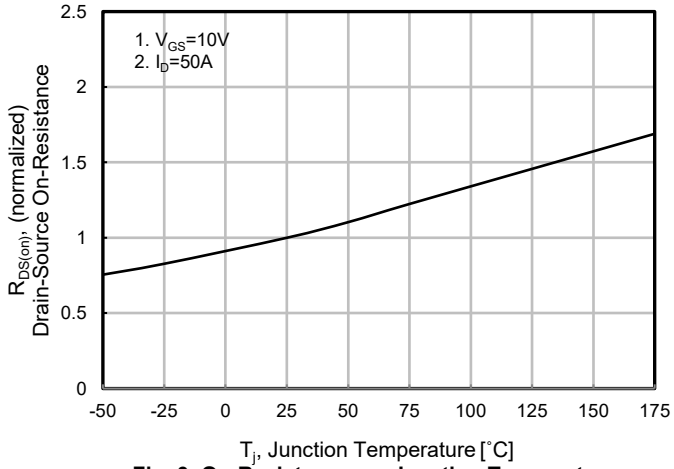


Fig. 3. On-Resistance vs. Junction Temperature

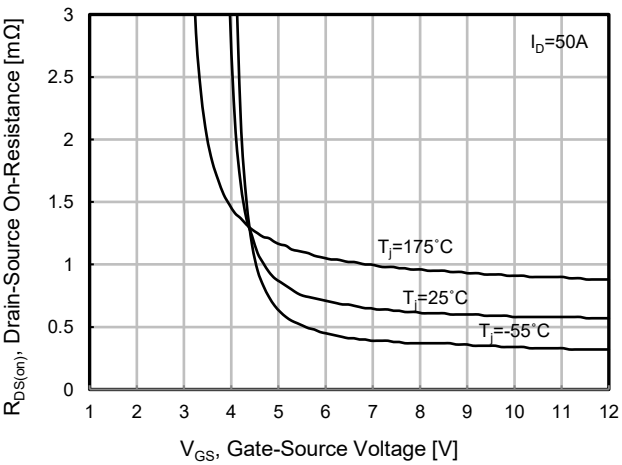


Fig. 4. On-Resistance vs. Gate-Source Voltage

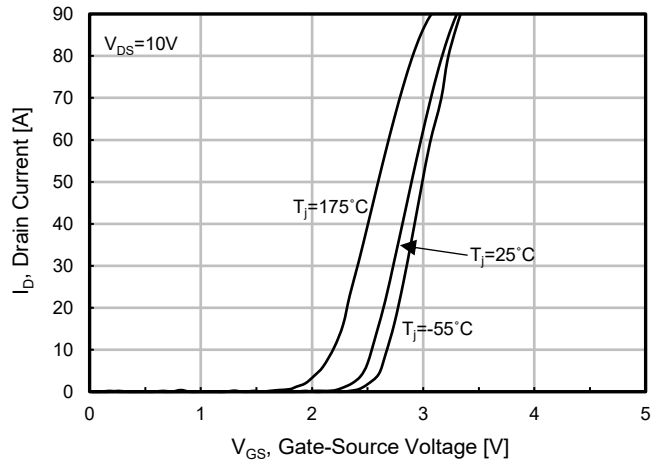


Fig. 5. Typ. Transfer Characteristics

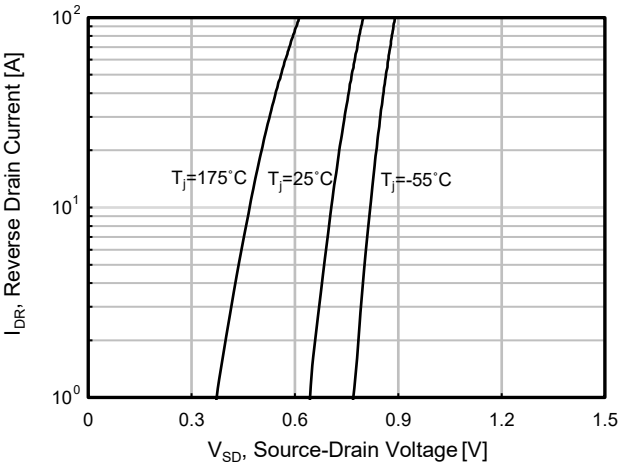


Fig. 6. Forward Characteristics of Reverse Diode

ELECTRICAL CHARACTERISTICS DIAGRAMS

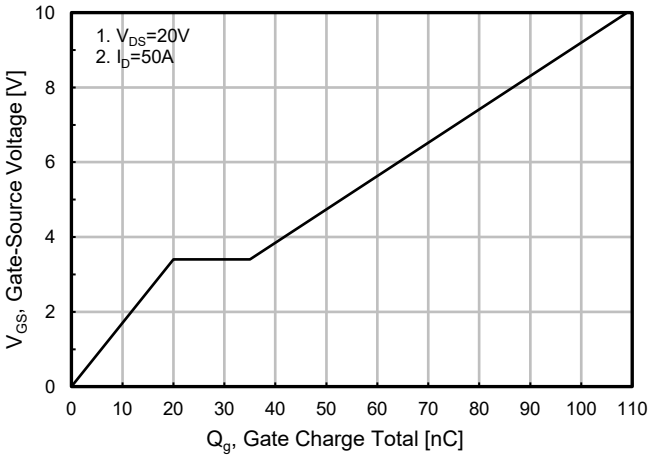


Fig. 7. Typ. Gate Charge

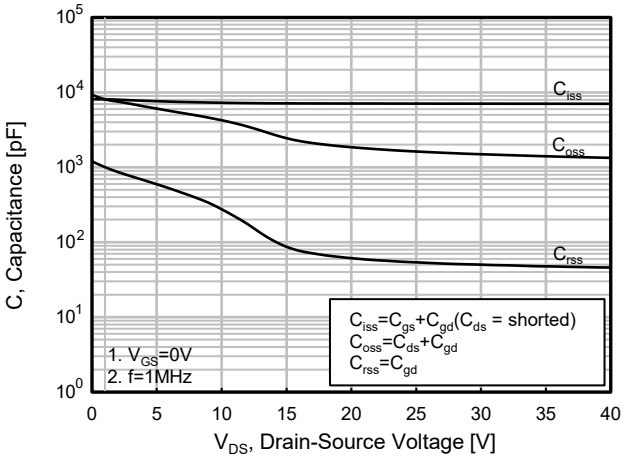


Fig. 8. Typ. Capacitance

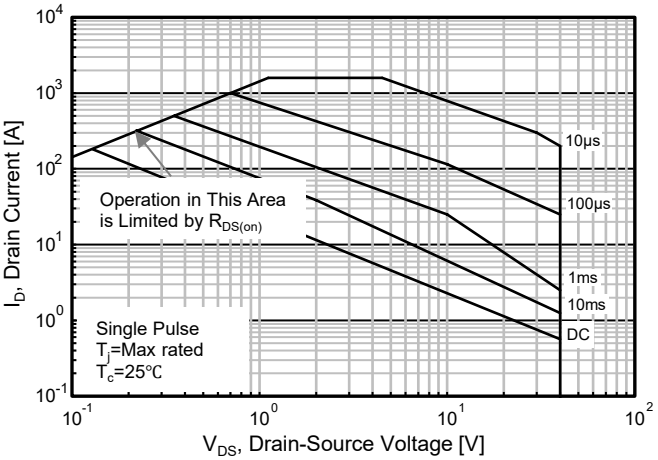


Fig. 9. Safe Operating Area

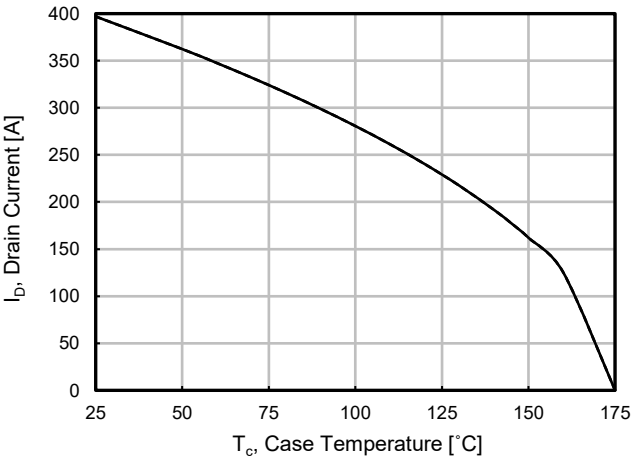


Fig. 10. Drain Current vs. Temperature

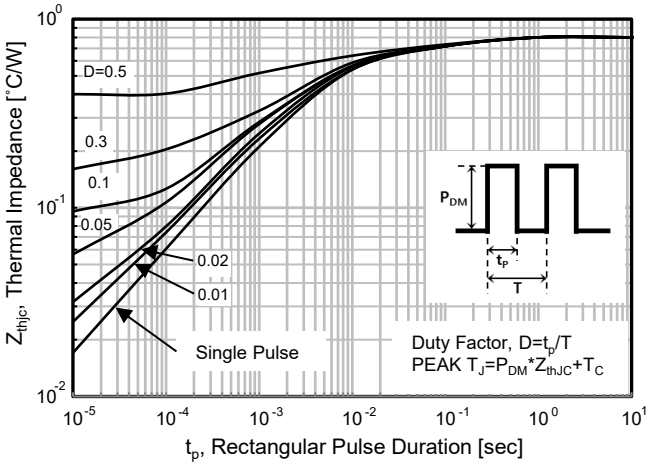


Fig. 11. Transient Thermal Impedence

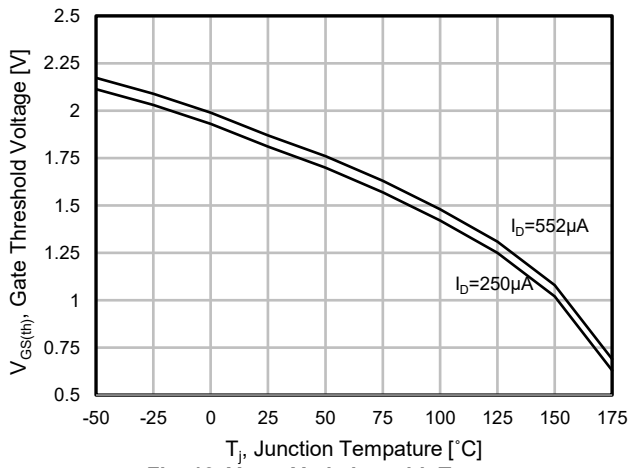


Fig. 12. $V_{GS(th)}$ Variation with Temperature

ELECTRICAL CHARACTERISTICS DIAGRAMS

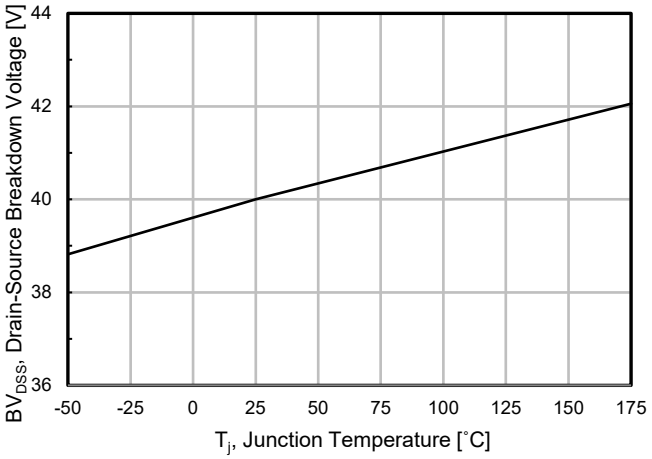


Fig. 13. BV_{DSS} Variation with Temperature

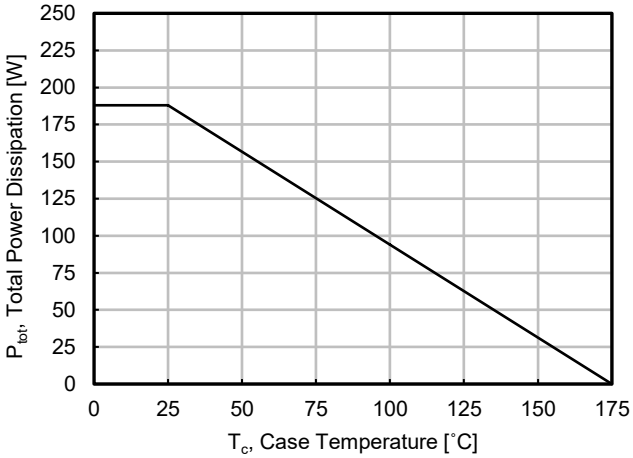
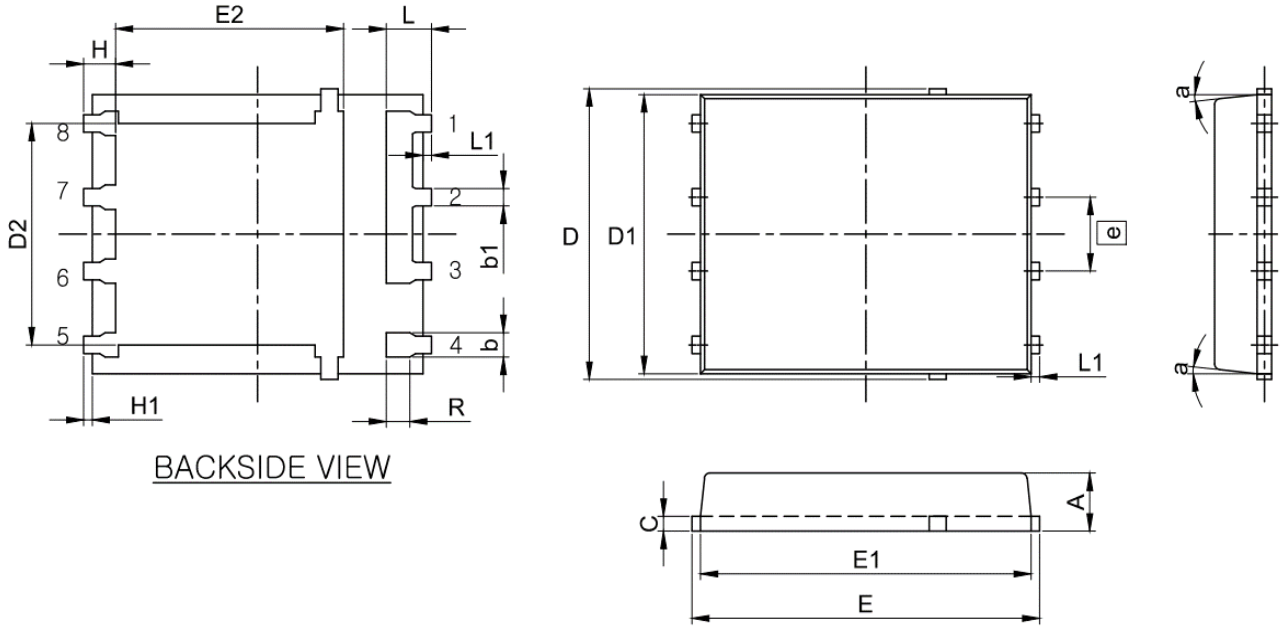


Fig. 14. Power Dissipation

Package Outlines

PDFN56



Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.90	–	1.10
b	0.33	–	0.49
b1	0.26	–	1.36
C	0.20	0.25	0.34
D	4.50	5.15	5.30
D1	4.50	5.00	5.10
D2	3.65	–	3.95
E	5.90	6.15	6.30
E1	5.85	6.00	6.10
E2	3.46	–	3.86
e	1.27 BSC		
H	0.50	–	0.71
H1	0.03	–	0.13
L	0.74	–	0.84
L1	0.03	–	0.13
R	0.48	–	0.58
a	0°	–	12°

Notes

Package body size, length and width do not include mold flash, protrusions and gate burrs.

DISCLAIMER :

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.