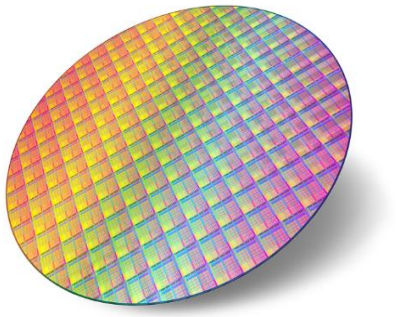
AMDW040N014VF

Single N-channel Trench MOSFET 40V 1.4mΩ

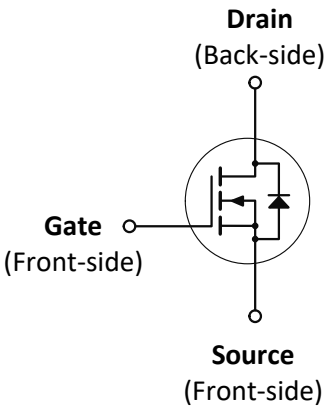
FEATURES

- **Trench power MOSFET technology**
- **N-channel, normal level**
- **Bare die (Sawn on Film)**
- **Maximum 175°C junction temperature**
- **AEC-Q101 qualified**



PRODUCT SUMMARY

V_{DS}	**40**	V
$R_{DS(on),\ typ.}$ (PDFN56)	**0.0011**	Ω
Die size	**2.9 x 3.6**	mm
Thickness (nom.)	**100**	μm



RoHS Compliant
HALOGEN-FREE

ABSOLUTE MAXIMUM RATINGS, at T_C = 25°C, unless otherwise sp

PARAMETER	SYMBOL	RATING	UNIT
Drain-source Voltage	V_{DS}	40	V
Gate-source Voltage	V_{GS}	± 20	V
Operating junction and storage temperature	T_j, T_{stg}	- 55 to +175	°C

ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
AMDW040N014VF	Bare Die	not defined	Sawn on Film	Halogen Free

http://www.magnachip.com

WAFER LEVEL ELECTRICAL TEST

at T_J = 25°C, unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=250 μA
Gate threshold voltage	$V_{GS(th)}$	2.35	3.10	3.85	V	V_{DS}=V_{GS}, I_D=250 μA
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=40 V, V_{GS}=0 V
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	V_{GS}=±20 V, V_{DS}=0 V
1) Drain-source on-state resistance	$R_{DS(on)}$	-	1.70	2.10	mΩ	V_{GS}=10 V, I_D=18 A
Diode forward voltage	V_{SD}	-	0.86	1.2	V	V_{GS}=0 V, I_S=18 A
2) Static DC Parameters When Packaged in PDFN56						
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=250 μA
Gate threshold voltage	$V_{GS(th)}$	2.35	3.10	3.85	V	V_{DS}=V_{GS}, I_D=250 μA
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=40 V, V_{GS}=0 V
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	V_{GS}=±20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.10	1.40	mΩ	V_{GS}=10 V, I_D=50 A
3) Forward transconductance	g_{fs}	-	130	-	S	V_{DS}=10 V, I_D=50 A
3) Dynamic Parameters						
Total gate charge	Q_g	-	71	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Gate-source charge	Q_{gs}	-	26	-		
Gate-drain charge	Q_{gd}	-	11	-		

MECHANICAL DATA

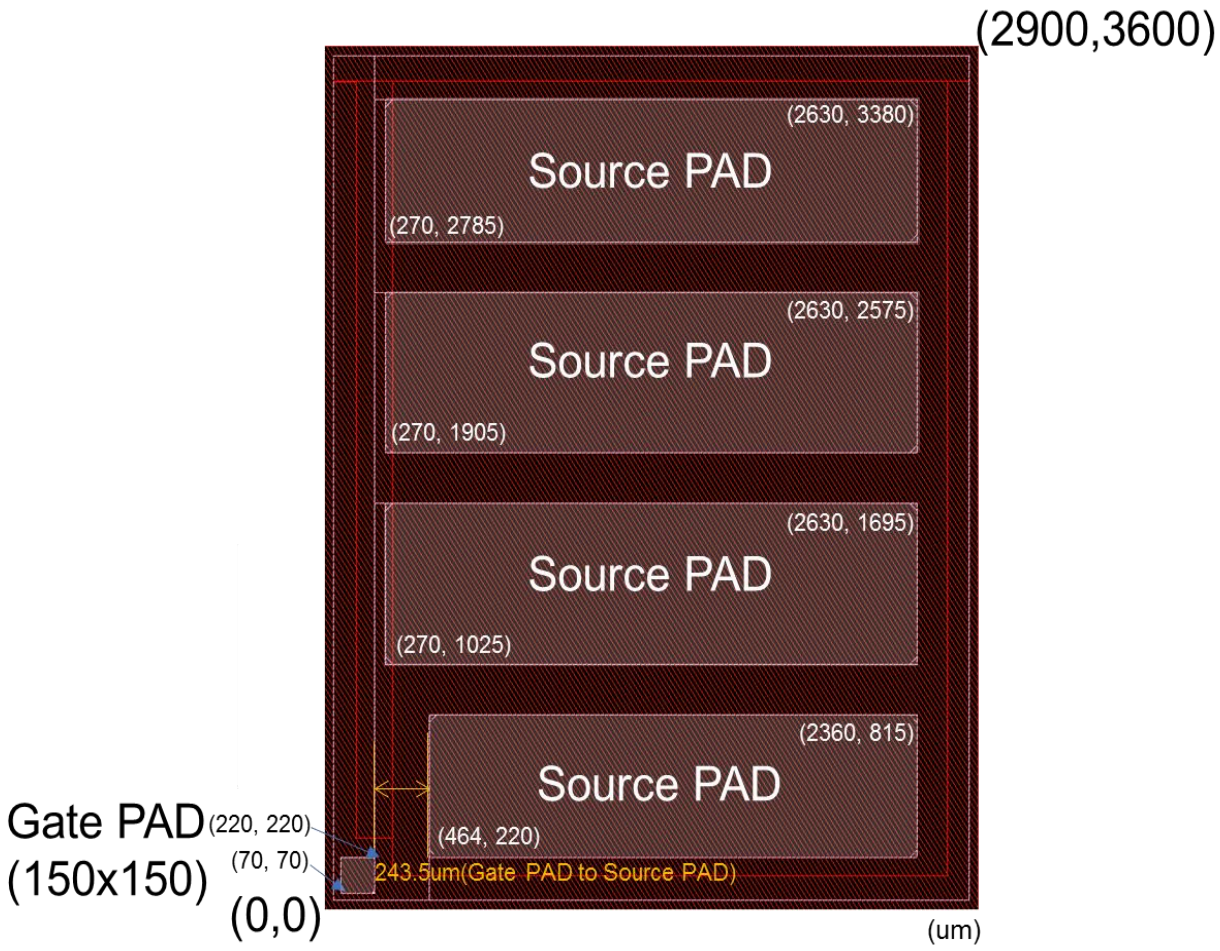
CONTENTS	CONFIGURATION
Passivation	Nitride (400 Å) / PSPI (5.5 μm)
Back Metal Composition (Thickness)	Ti (1,000 Å) – NiV (5,000 Å) – Ag (2,200 Å)
Front Metal Composition (Thickness)	Al (40,000 Å) – Ni-Au (10,550Å)
Die Dimension (with S/L)	2,900 μm x 3,600 μm
Gate Pad Dimension	150 μm x 150 μm
Wafer Diameter	200 mm, with 100 flat
Wafer Thickness	100 μm

Notes

1. Limited by wafer sort-equipment
2. When in PDFN56 package with solder die attach, Cu source clip, subject to final test conditions.
3. Guaranteed by design, not subject to production testing.

Die information

Wafer



DISCLAIMER :

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.