

MMD25R210RZ

250V 0.21Ω N-channel MOSFET

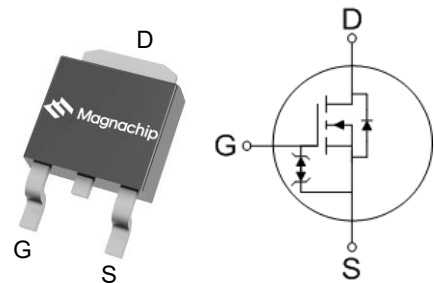
■ Description

MMD25R210RZ is power MOSFET using Magnachip's advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI and low switching loss as well as excellent ESD capability to designers.

■ Key Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	300	V
$R_{DS(on),max}$	0.21	Ω
$V_{TH,typ}$	3	V
I_D	13.8	A
$Q_{g,typ}$	17	nC

■ Package & Internal Circuit



■ Features

- Low power loss by high speed switching and low on-resistance
- 100% avalanche tested
- Green package – Pb free plating, halogen free
- Zener - integrated

■ Applications

- Switching applications
- DC-DC converters
- Motor control

■ Ordering Information

Order Code	Marking	Temp. Range	Package	Packing	RoHS Status
MMD25R210RZRH	25R210RZ	-55 ~ 150°C	TO-220	Reel	Compliant

■ Absolute Maximum Rating (T_c=25°C unless otherwise specified)

Parameter	Symbol	Rating	Unit	Note
Drain - source voltage	V _{DSS}	250	V	
Gate - source voltage	V _{GSS}	±25	V	
Continuous drain current ⁽¹⁾	I _D	13.8	A	T _C =25 °C
		8.7	A	T _C =100 °C
Pulsed drain current ⁽²⁾	I _{DM}	41.4	A	
Power dissipation	P _D	100	W	
Single - pulse avalanche energy ⁽³⁾	E _{AS}	350	mJ	
MOSFET dv/dt ruggedness	dv/dt	50	V/ns	
Diode dv/dt ruggedness ⁽⁴⁾	dv/dt	15	V/ns	
Storage temperature	T _{stg}	-55 ~150	°C	
Maximum operating junction temperature	T _j	150	°C	

- 1) I_D limited by maximum junction temperature
- 2) Pulse width t_p limited by T_{j,max}
- 3) L=18mH, I_{AS} = 6.5A, R_G = 25Ω
- 4) I_{SD} ≤ I_D, V_{DS peak} ≤ V_{(BR)DSS}

■ Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case max	R _{thjc}	1.25	°C/W
Thermal resistance, junction-ambient max	R _{thja}	40.6	°C/W

■ Static Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain - source breakdown voltage	$V_{(BR)DSS}$	250	-	-	V	$V_{GS} = 0V, I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1.0	μA	$V_{DS} = 250V, V_{GS} = 0V$
Gate leakage current	I_{GSS}	-	-	10	μA	$V_{GS} = \pm 25V, V_{DS} = 0V$
Drain - source on-state resistance	$R_{DS(on)}$	-	0.18	0.21	Ω	$V_{GS} = 10V, I_D = 6.5A$

■ Dynamic Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input capacitance	C_{iss}	-	627	-	pF	$V_{DS} = 100V, V_{GS} = 0V,$ $f = 400kHz$
Output capacitance	C_{oss}	-	52	-		
Reverse transfer capacitance	C_{riss}	-	8.3	-		
Effective output capacitance energy related ⁽⁵⁾	$C_{o(er)}$	-	58	-		
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{GS} = 10V, R_G = 25\Omega,$ $V_{DS} = 125V, I_D = 13.8A$
Rise time	t_r	-	27	-		
Turn-off delay time	$t_{d(off)}$	-	52	-		
Fall time	t_f	-	18	-		
Total gate charge	Q_g	-	17	-	nC	$V_{GS} = 10V, V_{DS} = 200V,$ $I_D = 13.8A$
Gate - source charge	Q_{gs}	-	3.5	-		
Gate - drain charge	Q_{gd}	-	8.1	-		
Gate resistance	R_G	-	13.1	-	Ω	$V_{GS} = 0V, f = 1MHz$

5) $C_{o(er)}$ is a capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0V to 80% $V_{(BR)DSS}$

■ Reverse Diode Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Continuous diode forward current	I_{SD}	-	-	13.8	A	
Diode forward voltage	V_{SD}	-	-	1.4	V	$I_{SD} = 13.8\text{A}$, $V_{GS} = 0\text{V}$
Reverse recovery time	t_{rr}	-	145	-	ns	$I_{SD} = 13.8\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 100\text{V}$
Reverse recovery charge	Q_{rr}	-	0.7	-	μC	
Reverse recovery current	I_{rrm}	-	10.0	-	A	

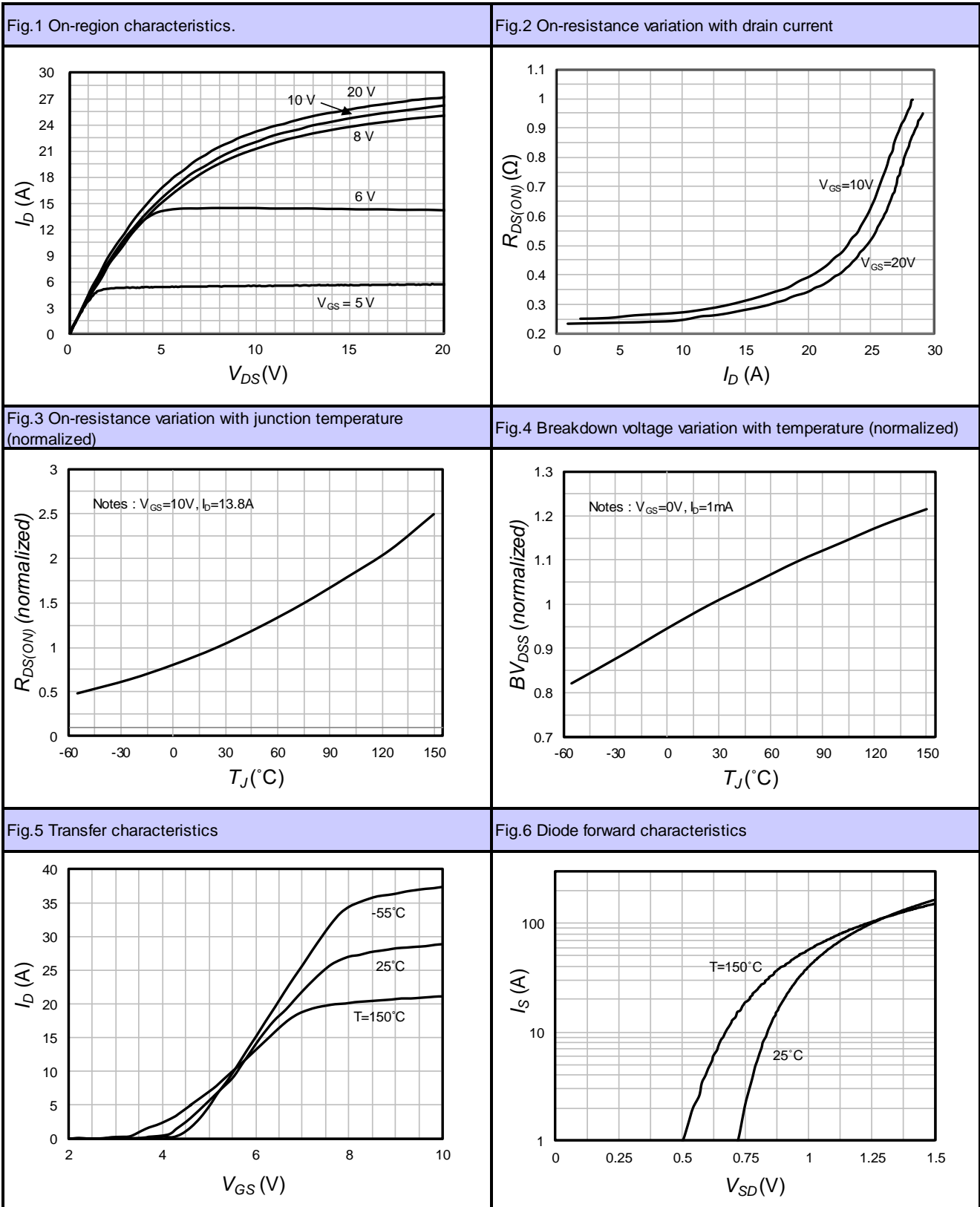
■ Characteristic Graph


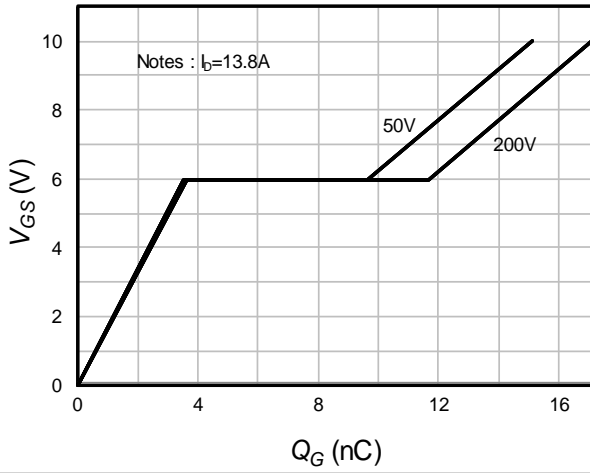
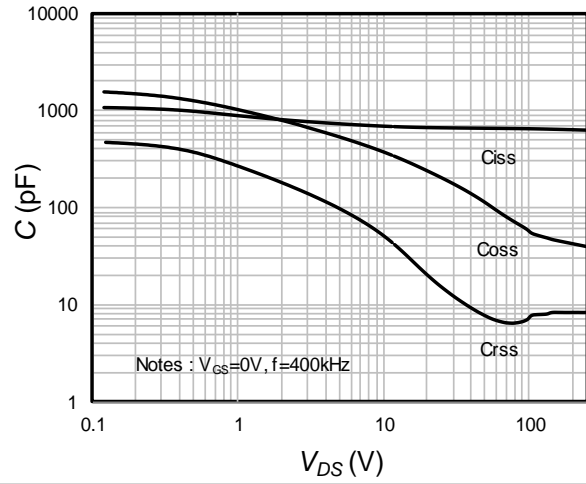
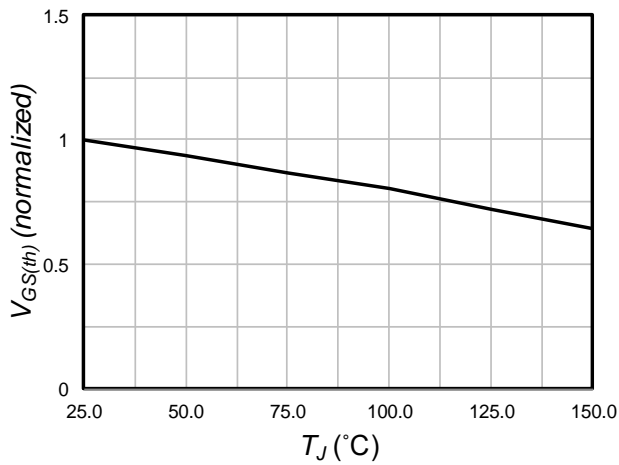
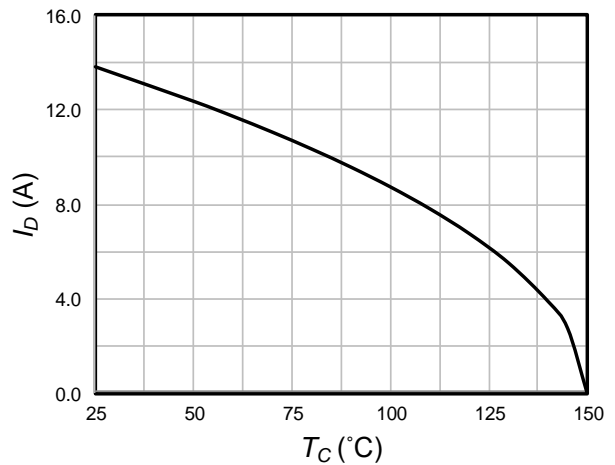
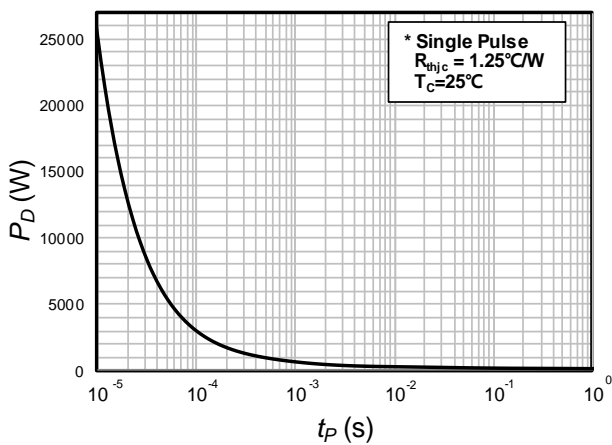
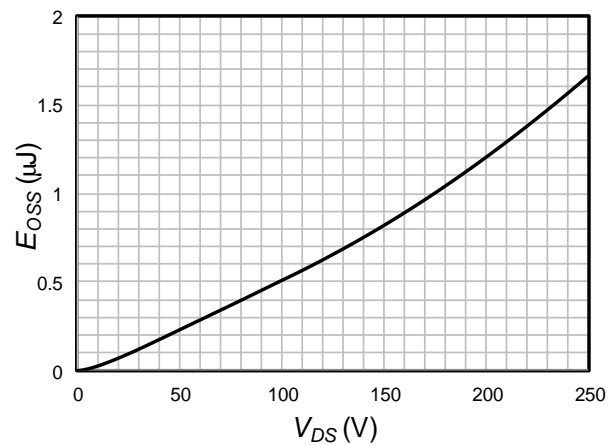
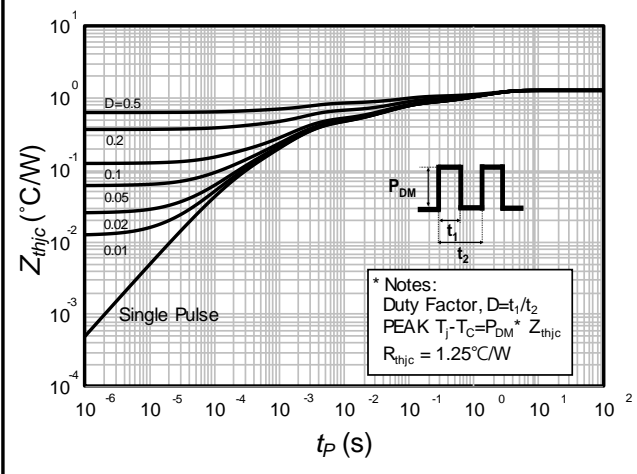
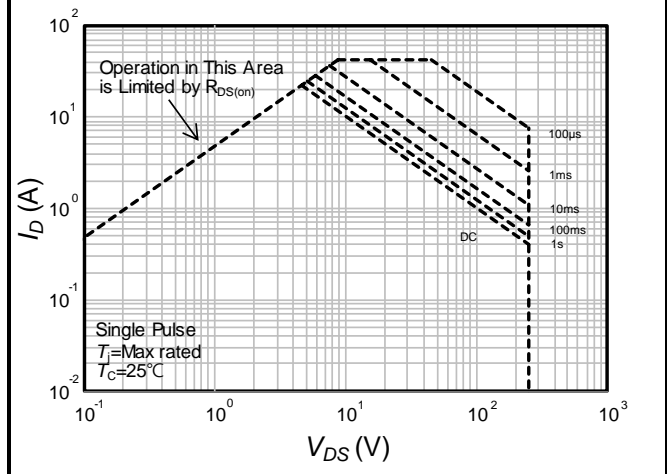
Fig.7 Gate charge characteristics

Fig.8 Capacitance characteristics

Fig.9 Threshold voltage variation with junction temperature

Fig.10 Drain current

Fig.11 Power dissipation variation with pulse time

Fig.12 Output capacitance stored energy


Fig.13 Transient thermal response

Fig.14 Safe operating area


■ Test Circuit

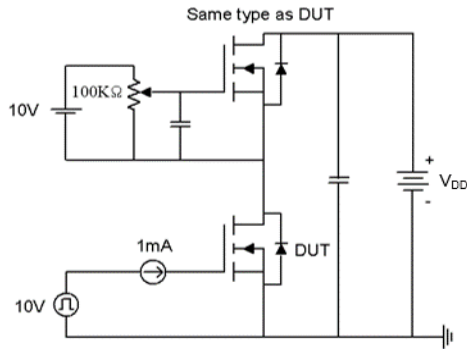


Fig15-1. Gate charge measurement circuit

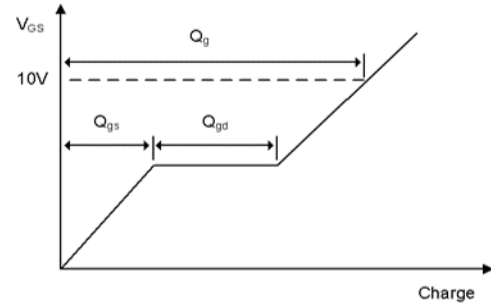


Fig15-2. Gate charge waveform

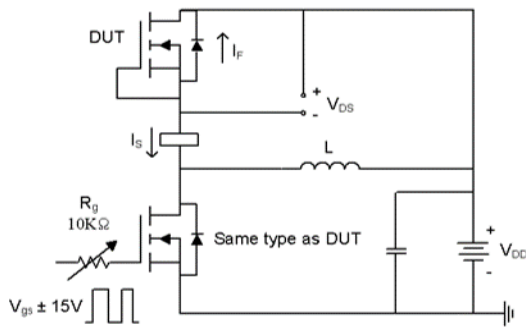


Fig16-1. Diode reverse recovery test circuit

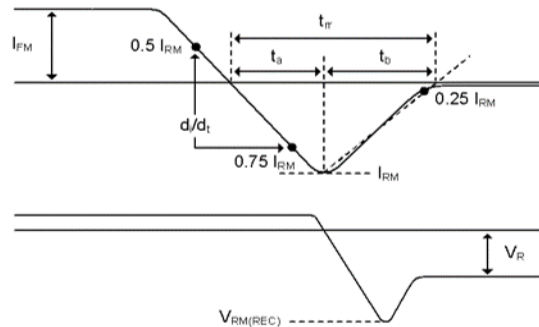


Fig16-2. Diode reverse recovery test waveform

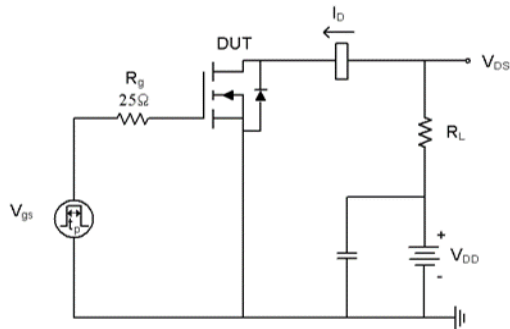


Fig17-1. Switching time test circuit for resistive load

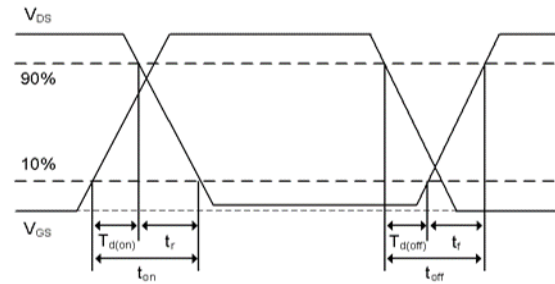


Fig17-2. Switching time waveform

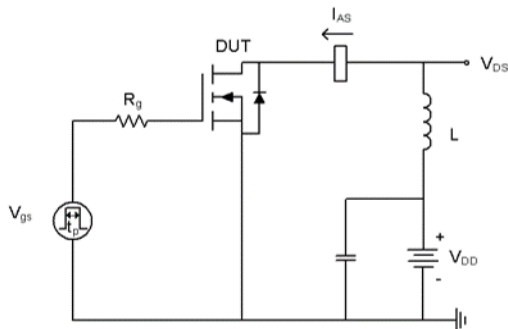


Fig18-1. Unclamped inductive load test circuit

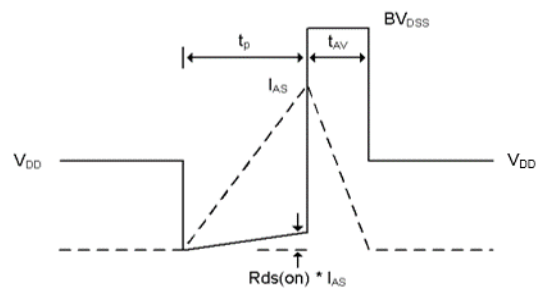
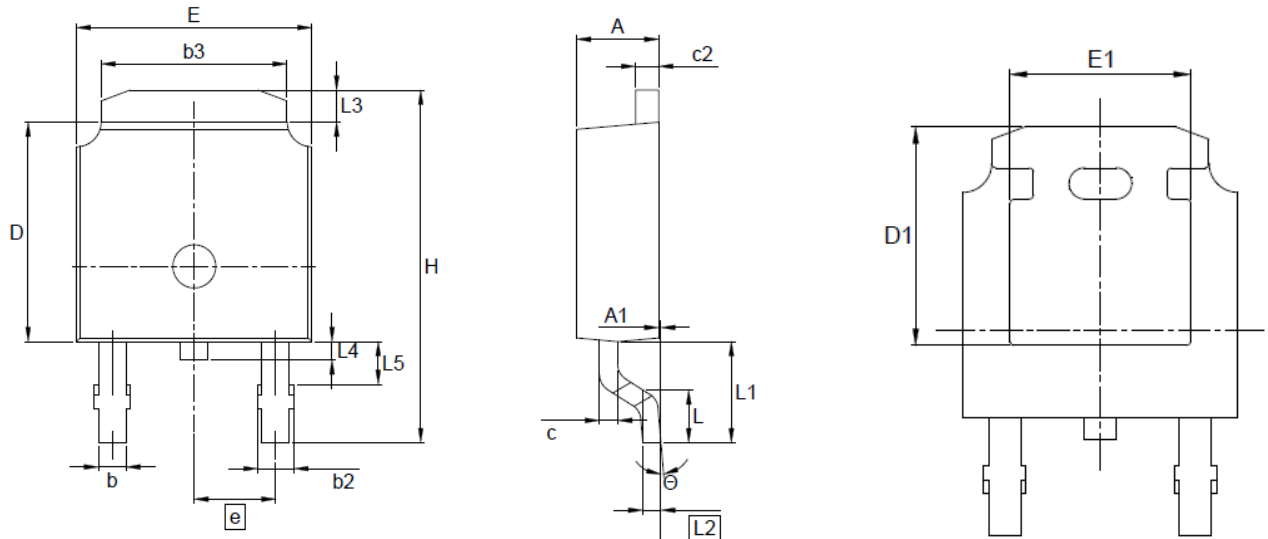


Fig18-2. Unclamped inductive waveform


■ Physical dimension
TO-252 (2L)


Note : Package body size, length and width do not include mold flash, protrusions and gate burrs

Symbol	Dimension (mm)		
	Min	Nom	Max
E	6,35	-	6,73
L	1,40	1,52	1,78
L1	2,74 REF		
L2	0,508 BSC		
L3	0,89	-	1,27
L4	-	-	1,02
L5	-	-	1,52
D	5,97	6,10	6,22
H	9,40	-	10,41
b	0,64	-	0,89
b2	0,76	-	1,14
b3	4,95	-	5,46
e	2,286 BSC		
A	2,18	-	2,39
A1	-	-	0,13
c	0,46	-	0,61
c2	0,46	-	0,89
D1	5,21	-	-
E1	4,32	-	-
θ	0°	-	10°

DISCLAIMER:

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

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