

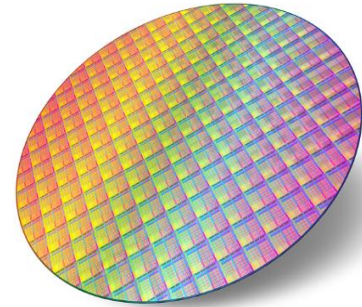


AMDW06N021F

Single N-channel Trench MOSFET 60V 2.1mΩ

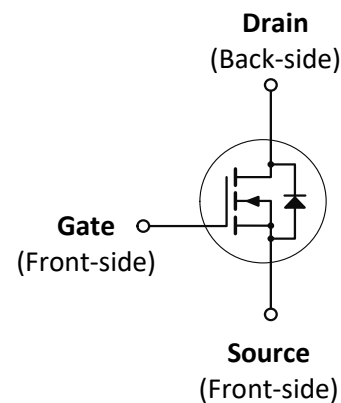
FEATURES

- Trench power MOSFET technology
- N-channel
- Bare die (Sawn on Film)
- Maximum 175°C junction temperature
- AEC-Q101 qualified



PRODUCT SUMMARY

V_{DS}	60	V
$R_{DS(on)}$, typ. (TO-247)	0.0021	Ω
Die size	4.0 x 7.2	mm
Thickness	200	μm



ABSOLUTE MAXIMUM RATINGS, at $T_C = 25^\circ\text{C}$, unless otherwise specified

PARAMETER	SYMBOL	RATING	UNIT
Drain-source Voltage	V_{DS}	60	V
Gate-source Voltage	V_{GS}	± 20	V
Operating junction and storage temperature	T_j, T_{stg}	- 55 to +175	$^\circ\text{C}$

ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
AMDW06N021F	Bare Die	not defined	Sawn on Film	Halogen Free

<http://www.magnachip.com>

WAFER LEVEL ELECTRICAL TEST at $T_J = 250^{\circ}\text{C}$, unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Static Parameters						
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=250\ \mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.5	2.3	3.1	V	$V_{DS}=V_{GS}$, $I_D=250\ \mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{ V}$, $V_{DS}=0\text{ V}$
1) Drain-source on-state resistance	$R_{DS(on)}$	-	2.1	2.8	m Ω	$V_{GS}=10\text{ V}$, $I_D=18\text{ A}$
		-	2.5	4.0		$V_{GS}=4.5\text{ V}$, $I_D=10\text{ A}$
Diode forward voltage	V_{SD}	-	0.8	1.2	V	$V_{GS}=0\text{ V}$, $I_S=18\text{ A}$

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
2) Static Parameters When Packaged in TO-247						
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=250\ \mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.5	2.3	3.1	V	$V_{DS}=V_{GS}$, $I_D=250\ \mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.1	-	m Ω	$V_{GS}=10\text{ V}$, $I_D=30\text{ A}$
		-	2.5	-		$V_{GS}=4.5\text{ V}$, $I_D=20\text{ A}$
3) Forward transconductance	g_{fs}	-	167	-	S	$V_{DS}=10\text{ V}$, $I_D=30\text{ A}$

3) Dynamic Parameters						
Input capacitance	C_{iss}	-	13272	-	pF	$V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$, $f=1.0\text{MHz}$
Output capacitance	C_{oss}	-	1254	-		
Reverse transfer capacitance	C_{rss}	-	662	-		
Total gate charge	Q_g	-	243	-	nC	$V_{DS}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$
Gate-source charge	Q_{gs}	-	48	-		
Gate-drain charge	Q_{gd}	-	64	-		

3) SOURCE-DRAIN DIODE						
Reverse recovery time	t_{rr}	-	83	-	ns	$I_F=30\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	195	-	nC	

MECHANICAL DATA

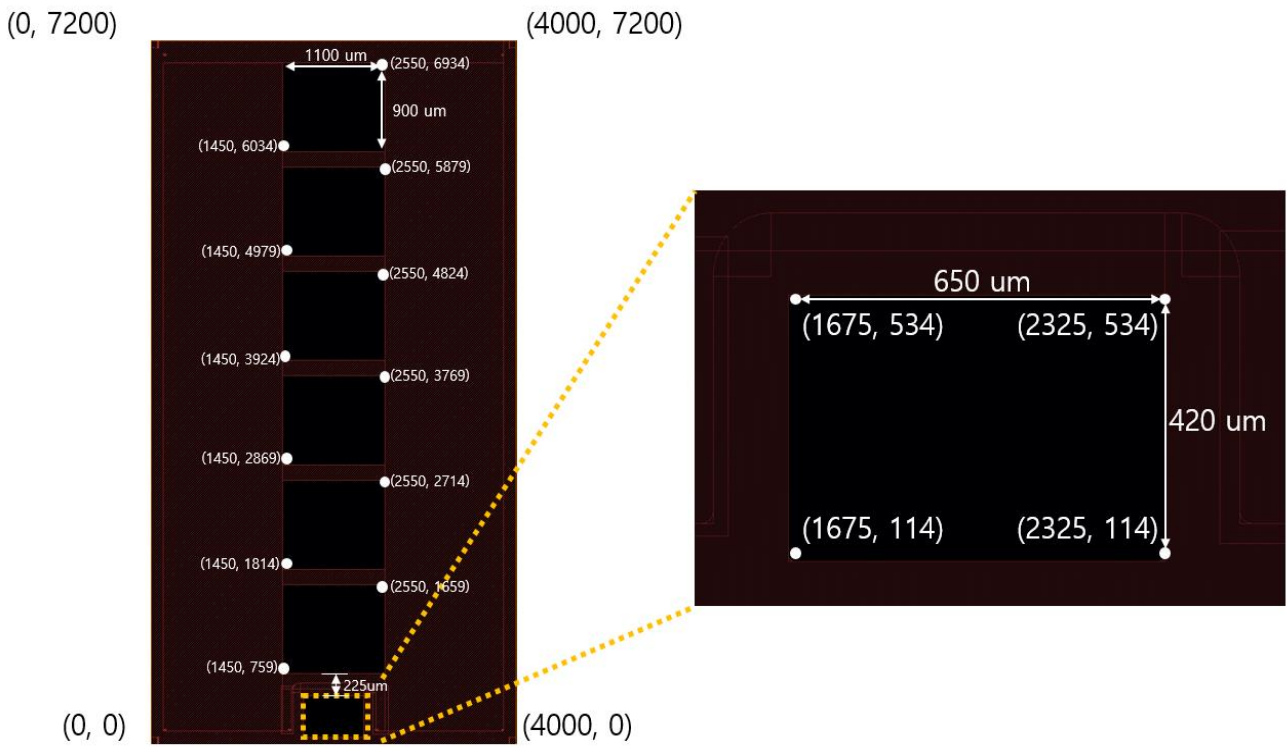
CONTENTS	CONFIGURATION
Passivation	Nitride (10,000 Å) / PSPI (5.5 μm)
Back Metal Composition (Thickness)	Ti (1,000 Å) – NiV (5,000 Å) – Ag (2,200 Å)
Front Metal Composition (Thickness)	Al (40,000 Å)
Die Dimension (with S/L)	4,000 μm x 7,200 μm
Gate Pad Dimension	650 μm x 420 μm
Wafer Diameter	200 mm, with 100 flat
Wafer Thickness	200 μm
Scribe lane width	80 μm

Notes

- Limited by wafer sort-equipment
- When in TO-247 package with 6 x 12 mil Al source wires, subject to final test conditions.
- Guaranteed by design, not subject to production testing.


Die information

Wafer



DISCLAIMER :

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

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