Magnachip

MAP8802B

CRM PFC Controller

General Description

The MAP8802B is an active power factor correction (PFC) controller for boost PFC applications that operates in critical conduction mode (CRM)

In CRM operation, the on time is constant during the ac line cycle and the off time varies with the instantaneous input voltage.

The voltage mode CRM PFC controller does not need the input voltage sense line. It can reduce power loss. CRM operation is an ideal choice for medium power (100W ~ 300W) PFC boost stages with the zero current switching of DCM operation.

MAP8802B provides protection functions such as overvoltage protection, under-voltage protection, open feedback loop protection, overcurrent protection, PFC output/bypass diode short protection, and ZCD winding short protection.

MAP8802B is available in an SOP-8 Pin package. The device operates over the -40°C ~ 125°C temperature.

Features

- Near Unity Power Factor
- No Input Voltage Sensing Requirement
- Latching PWM for Cycle-by-Cycle on time Control (Voltage Mode)
- Trans-conductance Amplifier
- High Precision Voltage Reference (±1.6% over the temperature range)
- Very low startup current consumption (≤ 35uA)
- Low typical operating current consumption
- Source 500mA / Sink 800mA Totem pole gate driver
- Under-voltage lockout with hysteresis
- Pin-to-Pin compatible with industry standards
- This is a Pb-Free and Halide-Free Device
- ZCD Short protection

Applications

- AC Adapter
- Ballast, Solid State Lighting
- LCD TV, Monitor
- PDP TV
- SMPS

Protection function

- Boost diode short Protection
- Bypass diode short Protection.
- ZCD winding short Protection
- Overvoltage Protection
- Overcurrent Protection
- Under-voltage Protection
- Open/Floating feedback Protection

Ordering Information

Part Number	Top Marking	Ambient Temperature Range	Package	Pb-Free
MAP8802B	MAP8802B	-40°C ~ 125°C	8-Lead Small Outline Package (SOP-8 Pin)	YES

Pin Configuration

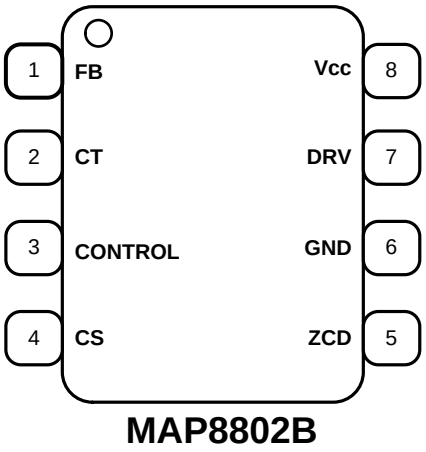


Figure 1. Pin configuration (Top View)

Pin Description

Pin NO	Name	Description
1	FB	The FB pin is the inverting input of the internal error amplifier. The output voltage of the boost PFC converter should be resistively divided to 2.5V.
2	CT	The CT pin sources a current to charge an external timing capacitor. The circuit controls the power switch on time by comparing the CT voltage to an internal voltage derived from $V_{CONTROL}$
3	CONTROL	The Control pin is the output of the internal error amplifier. A compensation network is connected between the control pin and ground to set the loop bandwidth.
4	CS	The CS pin limits the cycle-by-cycle current through the power switch. When the CS voltage exceeds V_{ILIM} , the drive turns off. The sense resistor that connects to the CS pin programs the maximum switch current.
5	ZCD	The ZCD pin is the zero current detection pin. When the voltage of this pin goes lower than 0.7V, the MOSFET is turned on.
6	GND	The GND pin is signal ground.
7	DRV	GATE driver output for external boost MOSFET
8	V_{CC}	The V_{CC} pin is the positive supply of the controller. The controller is enabled when V_{CC} exceeds $V_{CC(ON)}$ and is disabled when V_{CC} decreases to less than $V_{CC(OFF)}$.

Functional Block Diagram

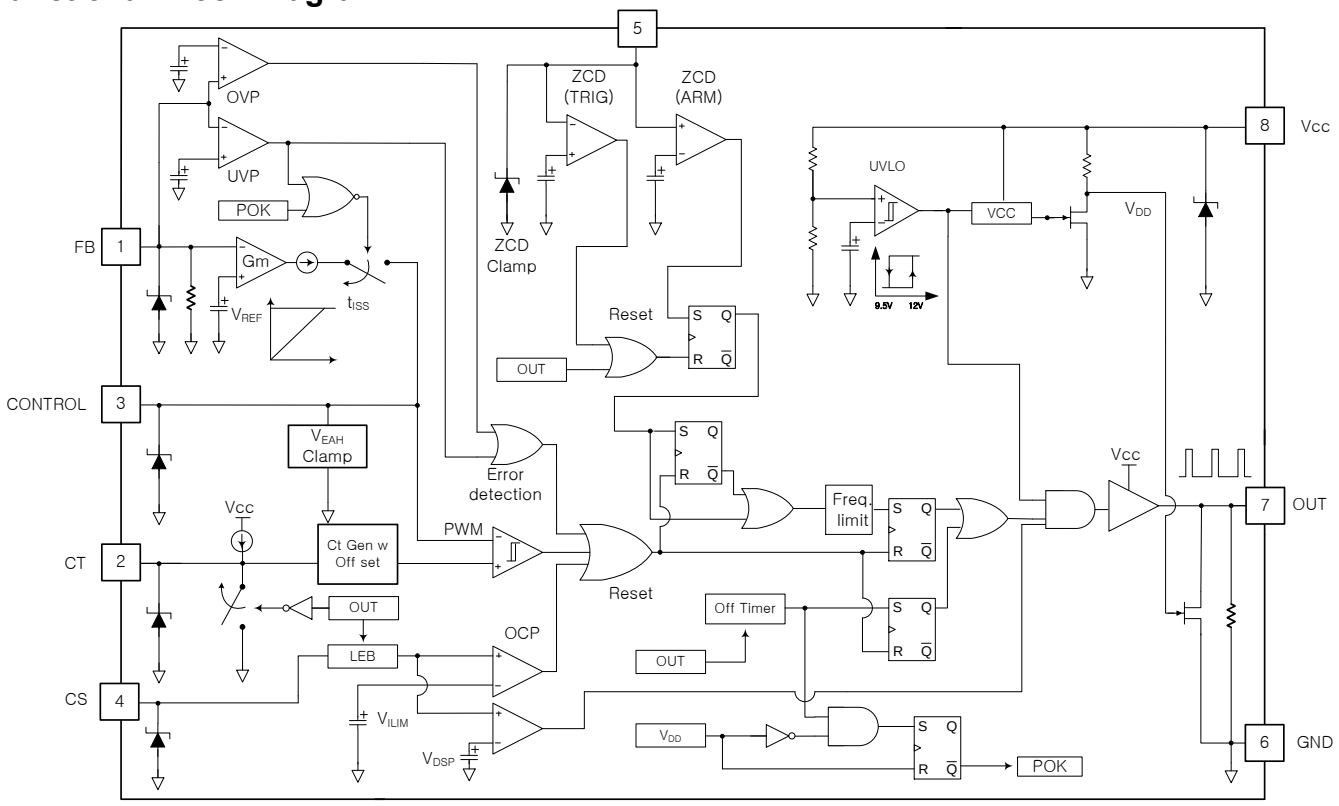


Figure 2. Block Diagram

Application Diagram

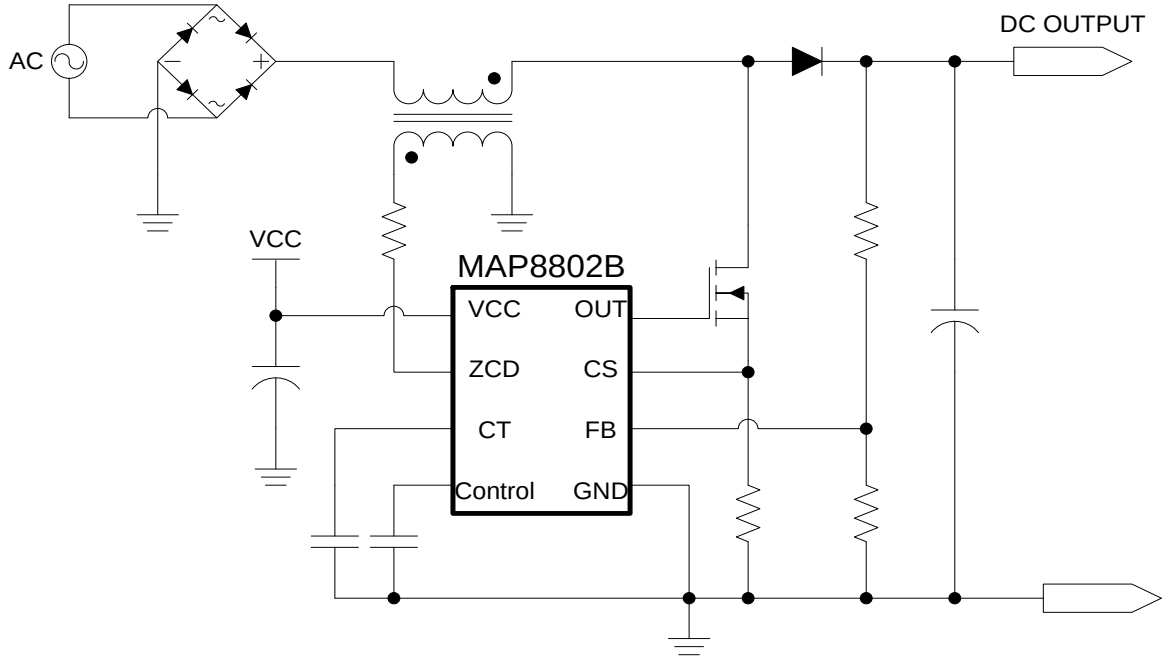


Figure 3. Typical Application

Absolute Maximum Ratings

Stresses exceeding Maximum Ratings may damage the device. Functional operation above the recommended operating conditions is not guaranteed. Extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	PARAMETER	VALUE	UNIT
V_{FB}	FB Voltage	-0.3 to 9	V
I_{FB}	FB Current	±10	mA
V_{CT}	Ct Voltage	-0.3 to 9	V
I_{CT}	Ct Current	±10	mA
$V_{CONTROL}$	Control Voltage	-0.3 to Vcontrol(clamp)	V
$I_{CONTROL}$	Control Current	-2 to 10	mA
V_{CS}	CS Voltage	-0.3 to 20	V
I_{CS}	CS Current	±10	mA
V_{ZCD}	ZCD Voltage	-0.3 to Vzcd(clamp)	V
I_{ZCD}	ZCD Current	±10	mA
V_{OUT}	OUT Voltage	-0.3 to V_{CC}	V
$I_{OUT(SINK)}$	OUT Sink Current	800	mA
$I_{OUT(SOURCE)}$	OUT Source Current	500	mA
V_{CC}	V_{CC} Supply Voltage	-0.3 to 20	V
I_{CC}	I_{CC} Supply Current	±20	mA
P_D	Power Dissipation(T_A = 70°C)	785	mW
$R_{\Theta JA}$	Thermal Resistance Junction-to-Ambient	101.9	°C/W
T_J	Operating Junction Temperature Range	-40 to 125	°C
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_L	Lead Temperature (Soldering, 10s)	300	°C
ESD	HBM on All Pins (1)	±5,000	V
	MM on All Pins (1)	±400	

Notes:

1. Human Body Model (HBM) per JESD22-A for all pins / Machine Model (MM) per JESD22-A 115 for all pins.

Electrical Characteristics

Unless noted, V_{CC} = 13V, and typical values are tested at T_A = 25°C

Symbol	Characteristic	Conditions	Min	Typ	Max.	Unit
STARTUP AND SUPPLY CIRCUITS						
$V_{CC(ON)}$	Startup Voltage Threshold	V_{CC} Increasing	11	12	13	V
$V_{CC(OFF)}$	Minimum Operating Voltage	V_{CC} Decreasing	8.8	9.5	10.2	V
H_{UVLO}	Supply Voltage Hysteresis		-	2.5	-	V
$I_{CC(Startup)}$	Startup Current Consumption	0V < V_{CC} < $V_{CC(ON)}$ -200mV	-	24	35	µA
I_{CC1}	No Load Switching Current Consumption	C_{OUT} = open, 70kHz Switching, V_{CS} = 0V	-	1.4	1.7	mA
I_{CC2}	Switching Current Consumption	C_{OUT} = 1nF, 70kHz Switching, V_{CS} = 0V	-	2.4	2.9	mA
$I_{CC(fault)}$	Fault Condition Current Consumption	No Switching, V_{FB} = 0V	-	1.2	1.45	mA
ERROR AMPLIFIER SECTION						
V_{REF}	Voltage Reference	T_A = 25°C	2.475	2.500	2.525	V
$\triangle V_{REF1}$	Voltage Reference Line Regulation	$V_{CC(ON)}$ + 200mV < V_{CC} < 20V	-10	-	10	mV
$\triangle V_{REF2}$	Temperature Stability of V_{REF} (2)		-1.6	-	1.6	%
I_{EA} (SINK/SOURCE) $I_{EA(SINK)OVP}$	Error Amplifier Current Capability	V_{FB} = V_{REF} ±0.1V V_{FB} = 1.08 * V_{REF} or V_{REF} + 0.2V	6 20	10 50	20 80	uA
Gm	Trans conductance	V_{FB} = V_{REF} ±0.1V V_{FB} > V_{REF} + 0.2V, V_{FB} < V_{REF} - 0.2V	105 -	125 250	145 -	µmho
R_{FB}	Feedback Pin Internal Pull Down Resistor	V_{FB} = V_{UVP} to V_{REF}	2	4.6	10	MΩ
I_{FB}	Feedback Bias Current	V_{FB} = 2.5V	0.25	0.54	1.25	µA
$I_{CONTROL}$	Control Bias Current	V_{FB} = 0V	-1	-	1	µA
V_{EAH}	Maximum Control Voltage	$I_{CONTROL(PULL\ UP)}$ = 10uA, V_{FB} > V_{REF} (V_{FB} = V_{REF} + 0.1V)	5	5.5	6	V
$Ct_{(offset)}$	Minimum Control Voltage to Generate output Pulses	$V_{CONTROL}$ = Decreasing until V_{OUT} is low, V_{CT} = 0V	0.37	0.65	0.88	V
$V_{EA(DIFF)}$	Control Voltage Range	V_{EAH} – $Ct_{(offset)}$	4.5	4.9	5.3	V
CURRENT SENSE SECTION						
t_{LEB}	Leading Edge Blanking Duration	V_{CS} = 0V, V_{OUT} = 90% to 10%	100	190	350	ns
t_{CS}	Overcurrent Detection Propagation Delay	dV/dt = 10V/us V_{CS} = V_{ILIM} to V_{OUT} = 10%	40	100	170	ns
I_{CS}	Current Sense Bias Current	V_{CS} = 2V	-1	-	1	µA

Electrical Characteristics

Unless noted, V_{CC} = 13V, and typical values are tested at T_A = 25°C

Symbol	Characteristic	Conditions	Min	Typ	Max.	Unit
RAMP CONTROL SECTION						
$V_{Ct(MAX)}$	Ct Peak Voltage	$V_{Control}$ = open	4.575	4.93	5.025	V
I_{Charge}	Ontime Capacitor Charge Current (2)	$V_{Control}$ = open V_{Ct} = 0V to $V_{Ct(MAX)}$	235	275	297	µA
$t_{Ct(Discharge)}$	Ct Capacitor Discharge Duration (2)	$V_{Control}$ = open V_{Ct}=$V_{Ct(MAX)}$ – 100mV to 500mV	-	50	150	ns
t_{PWM}	PWM Propagation Delay (2)	dV/dt = 30V/us V_{Ct} = $V_{Control}$ – Ct $_{(offset)}$ to V_{OUT} = 10%	-	130	220	ns
MAX FREQUENCY LIMIT SECTION						
f_{MAX}	Maximum Switching Frequency		-	300	400	kHZ
ZERO CURRENT DETECTON						
$V_{ZCD(ARM)}$	ZCD Arming Threshold	V_{ZCD} = Increasing	1.25	1.4	1.55	V
$V_{ZCD(TRIG)}$	ZCD Triggering Threshold	V_{ZCD} = Decreasing	0.6	0.7	0.83	V
$V_{ZCD(HYS)}$	ZCD Hysteresis		-	700	-	mV
I_{ZCD}	ZCD Bias Current	V_{ZCD} = 5V	-2	-	+2	µA
$V_{CL(POS)}$	Positive Clamp Voltage	I_{ZCD} = 3mA	4.5	6	7.5	V
$V_{CL(NEG)}$	Negative Clamp Voltage	I_{ZCD} = -2mA	-0.9	-0.7	-0.5	V
t_{ZCD}	ZCD Propagation Delay	V_{ZCD} = 2V to 0V ramp, dV/dt = 20V/us V_{ZCD} = $V_{ZCD(TRIG)}$ to V_{OUT} = 90%	-	100	170	ns
t_{SYNC}	Minimum ZCD Pulse Width (2)		-	70	-	ns
t_{Start}	Maximum Off Time in Absence of ZCD Transition	Falling V_{OUT} = 10% to Rising V_{OUT} = 90%	75	165	300	µs
OUTPUT SECTION						
R_{OH} R_{OL}	Output Resistance (2)	I_{SOURCE} = 100mA I_{SINK} = 100mA	- -	12 6	20 13	Ω
t_{rise}	Rise Time	10% to 90%	-	35	80	ns
t_{fall}	Fall Time	90% to 10%	-	25	70	ns
$V_{DRV(start)}$	Output Low Voltage	V_{CC} =$V_{CC(ON)}$ – 200mV, I_{SINK} = 10mA	-	-	0.2	V
PROTECTION						
V_{ILIM}	Current Sense Voltage Threshold (4)		0.45	0.5	0.55	V
V_{OVP}	Overvoltage Detect Threshold	V_{FB} = Increasing	104	106	108	%
$V_{OVP(HYS)}$	Overvoltage Hysteresis		20	50	90	mV
t_{OVP}	Overvoltage Detect Threshold Propagation Delay (2)	V_{FB} = 2V to 3V ramp, dV/dt = 1V/us V_{FB} = V_{OVP} to V_{OUT} = 10%	-	500	800	ns
V_{UVP}	Undervoltage Detect Threshold	V_{FB} = Decreasing	0.23	0.31	0.4	V
t_{UVP}	Undervoltage Detect Threshold Propagation Delay (2)	V_{FB} = 1V to 0V ramp, dV/dt = 10V/us V_{FB} = V_{UVP} to V_{OUT} = 10%	100	200	300	ns
V_{DSP}	Diode short protection (3) (4)			2.4		V

Notes:

2. This parameters are not production tested: Guaranteed by design correlation.
3. This parameter is influenced by board pattern. So we are recommended that connect to bid at MOSFET drain current path.

4. This parameter is reflects LEB.

Typical Operating Characteristics

Unless noted, V_{CC} = 13V, and typical values are tested at T_A = 25°C

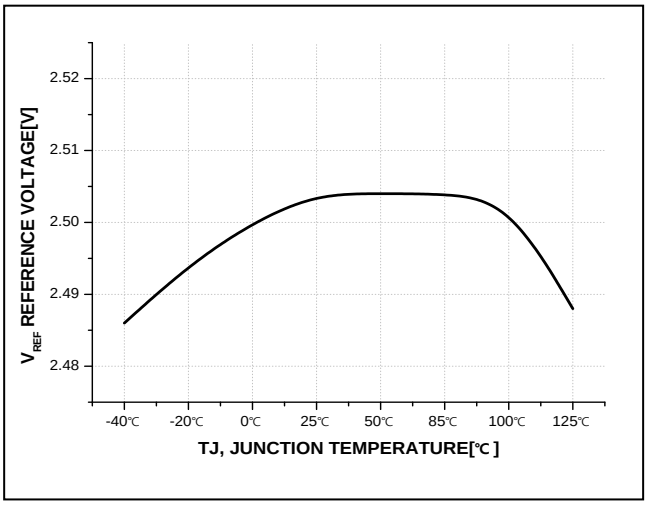


Figure 4. Reference Voltage vs. Junction Temperature

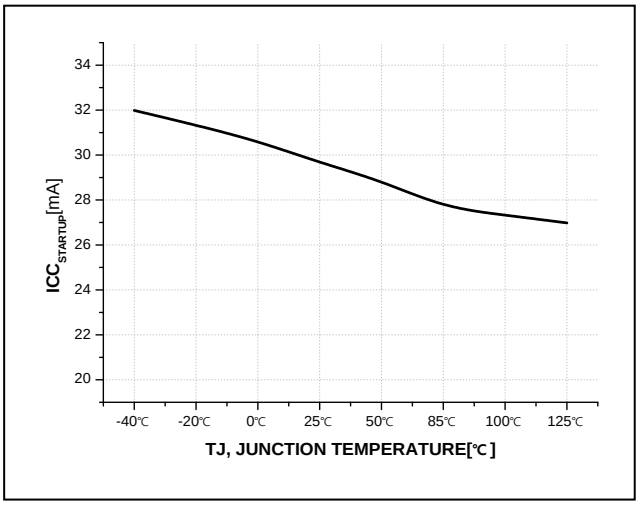


Figure 5. Startup Current Consumption vs. Junction Temperature

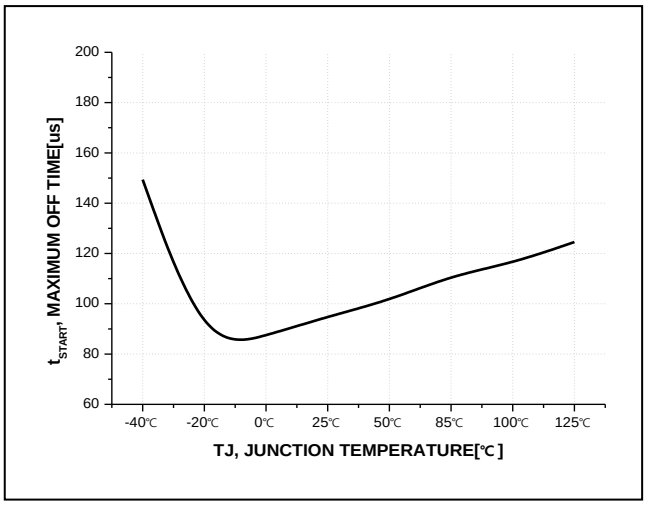


Figure 6. Maximum off time in Absence of ZCD Transition vs. Junction Temperature

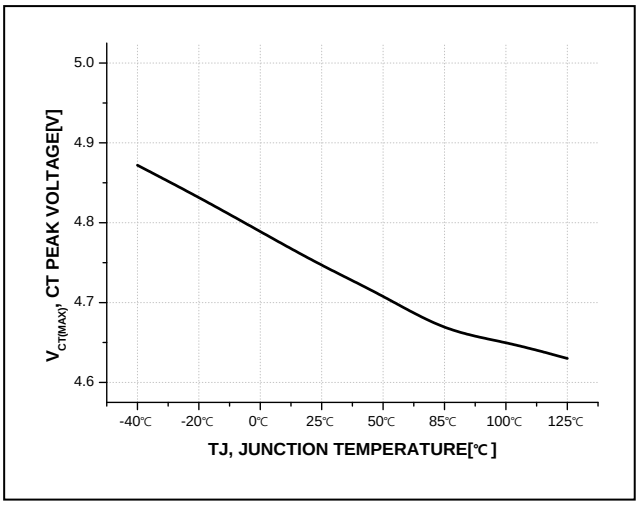


Figure 7. Ct Peak Voltage vs. Junction Temperature

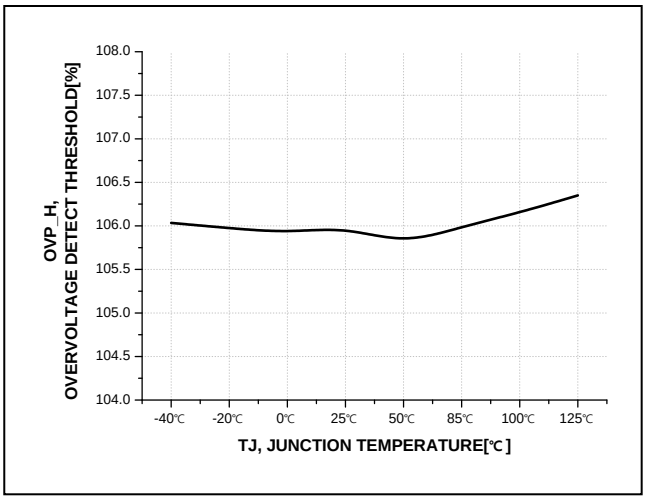


Figure 8. Overvoltage High Detect Threshold vs. Junction Temperature

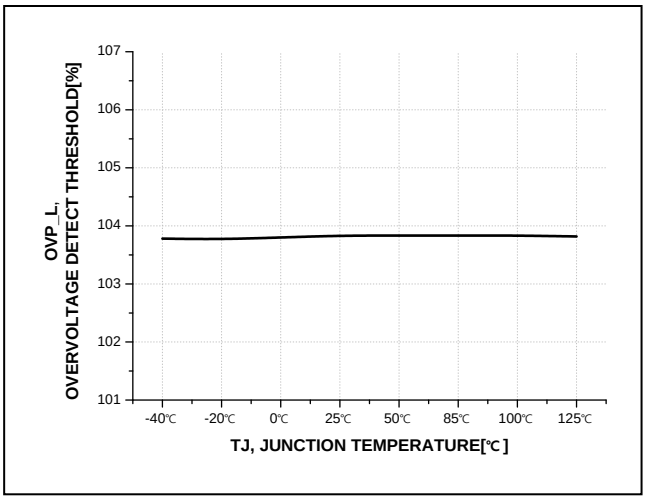


Figure 9. Overvoltage Low Detect Threshold vs. Junction Temperature

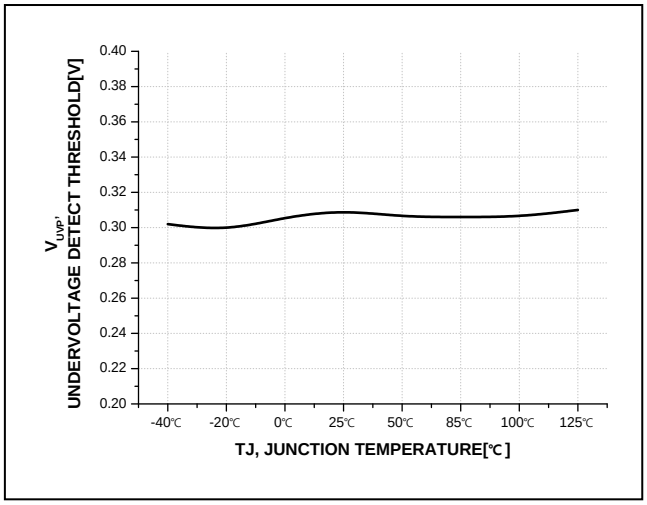


Figure 10. Undervoltage Detect Threshold vs. Junction Temperature

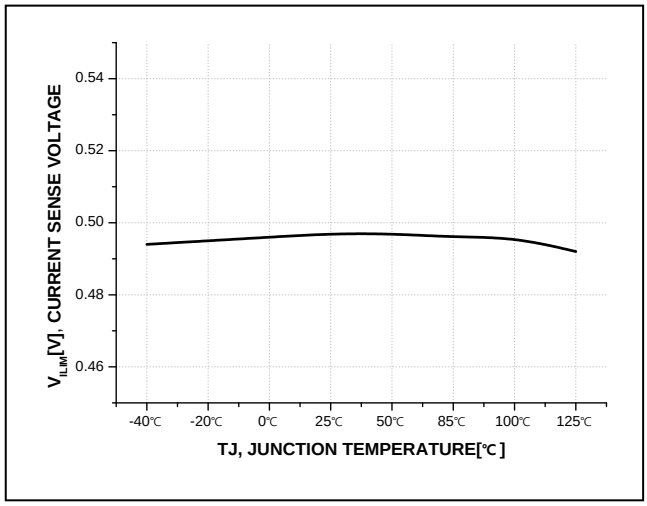


Figure 11. Current Sense Voltage Threshold vs. Junction Temperature

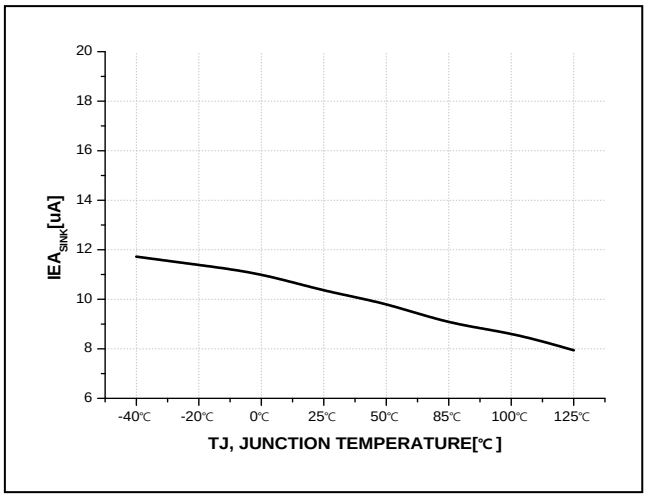


Figure 12. Error Amplifier Sink Current vs. Junction Temperature

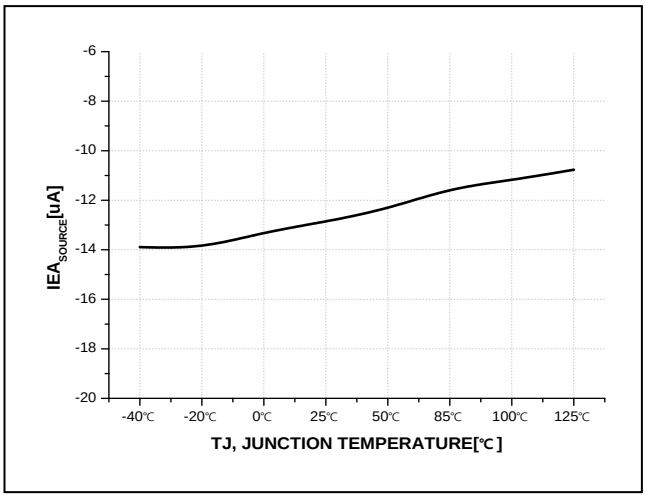


Figure 13. Error Amplifier Source Current vs. Junction Temperature

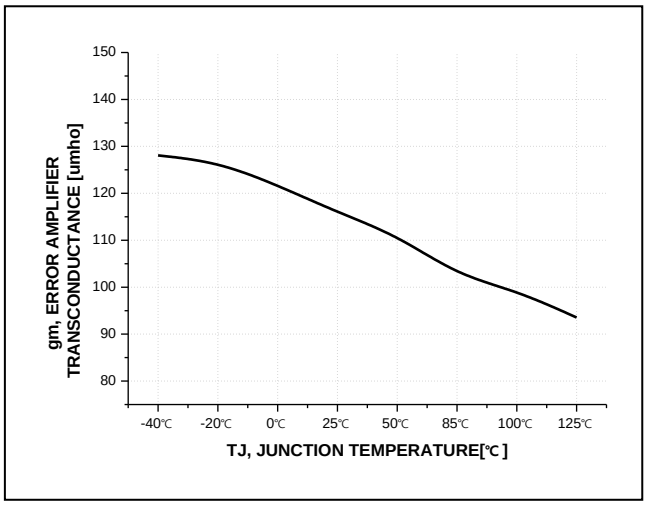


Figure 14. Error Amplifier Transconductance vs. Junction Temperature

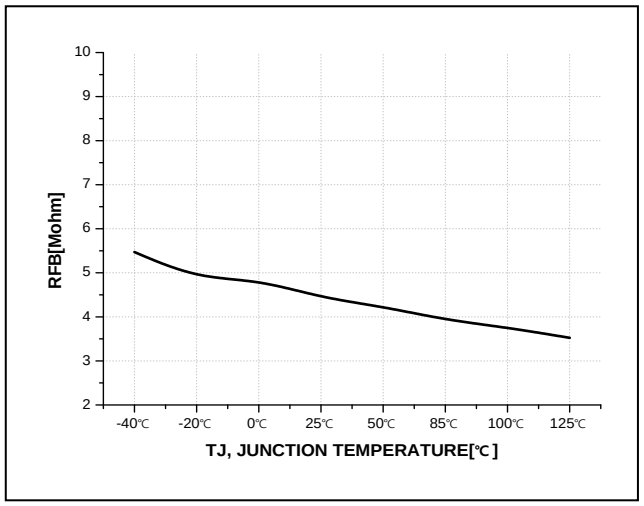


Figure 15. Feedback Pin Internal Pull-Down Resistor vs. Junction Temperature

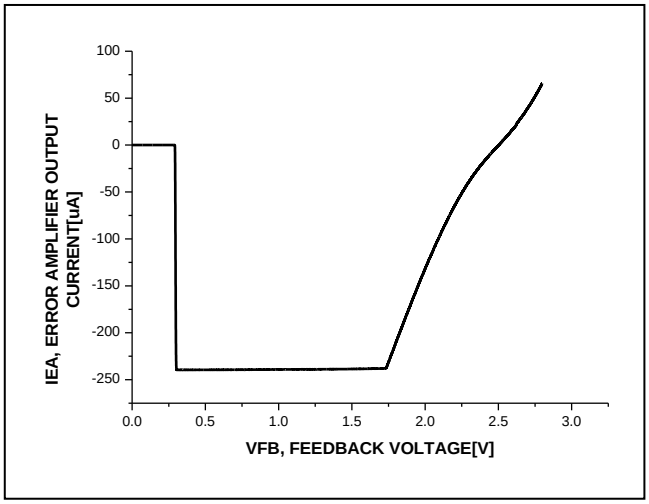


Figure 16. Error Amplifier Output Current vs. Feedback Voltage

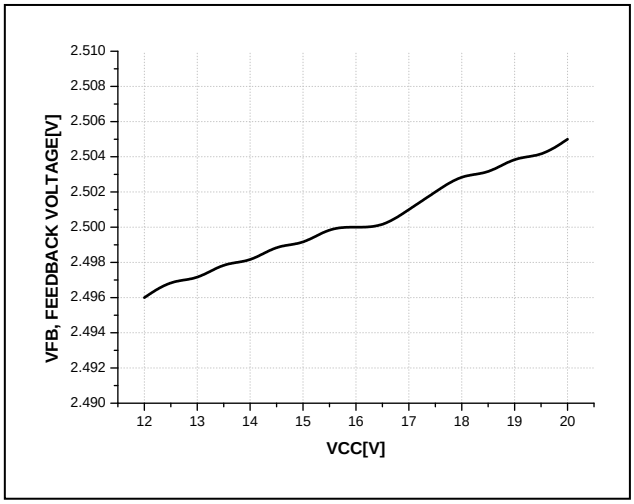


Figure 17. Feedback Voltage vs. VCC Voltage

Application Information

1. Start up

Generally, if the V_{CC} voltage goes to $V_{CC(ON)}$, the IC's internal blocks are enabled. The low startup current consumption (<35uA) enables minimized standby power dissipation. The V_{CC} voltage should be higher than 9.5V under normal conditions after start-up.

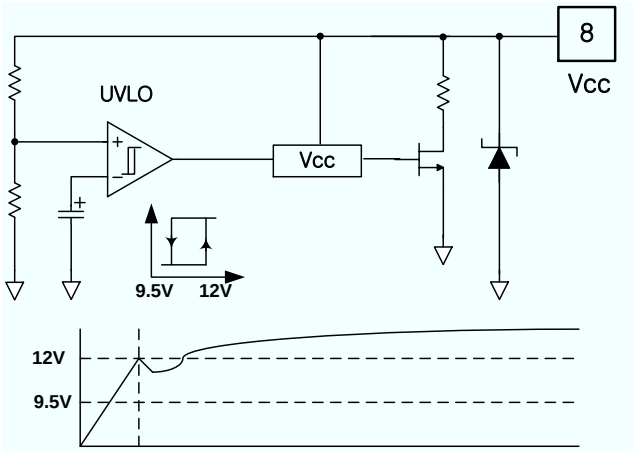


Figure 18. Startup circuit

2. FB Block

Scaled-down voltage from the output is the input for the FB pin. The used trans-conductance amplifier is good for the implementation of OVP and disables functions. The output current of the amplifier varies according to the voltage difference. The MAP8802B features comprehensive protection against open feedback loop conditions by including OVP, UVP, and FBP. Figure 19 illustrates three conditions in which the feedback loop is open.

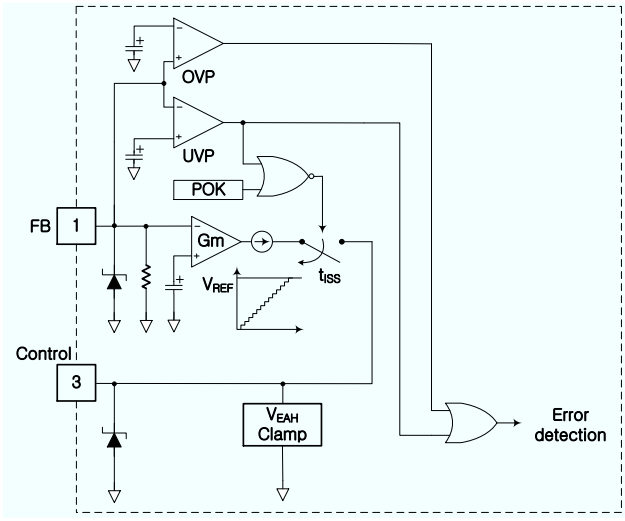


Figure 19. Open Feedback Loop Protection

The **UVP** comparator detects an UVP fault, the drive and error amplifier are disabled.
The **OVP** comparator detects an OVP fault and the drive is disabled.

The **FB** is floating. The internal pull down resistor R_{FB} pulls down the FB voltage below V_{UVP}. The UVP comparator detects an UVP fault, the drive and error amplifier are disabled.

3. Ct Block

The MAP8802B controls the on time with the capacitor connected to the Ct pin. A current source charges the Ct capacitor to a voltage derived from the Control pin voltage ($V_{Ct(off)}$). When $V_{Ct(off)}$ is reached, the drive turns off.(Figure 20. Turn on Time Regulation) The Ct capacitor is sized to ensure that the required on time is reached at maximum output power and the minimum input voltage condition. The Ct pin discharges the external timing capacitor at the end of the on time.

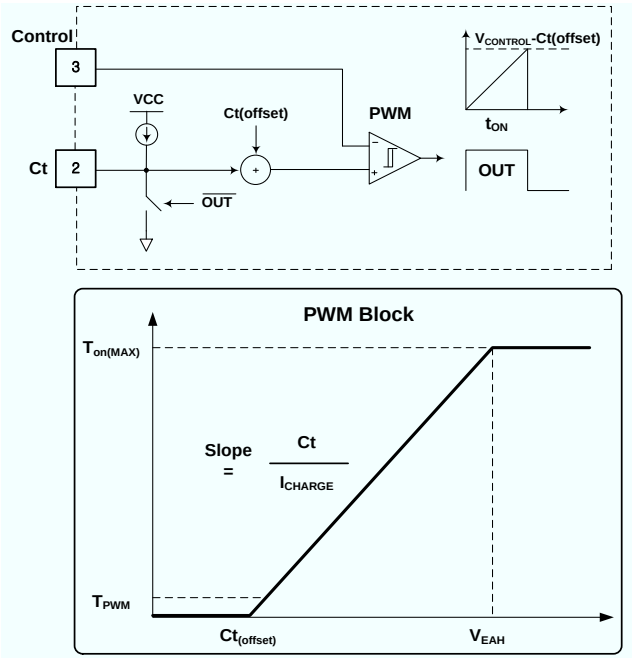


Figure 20. Turn on Time Regulation

4. Control Block

The scaled output is compared with the internal reference voltage and sinking or sourcing current is generated from the control pin by a trans-conductance amplifier. The error amplifier output is compared with the saw-tooth waveform created at the Ct. When load is heavy, output voltage decreases, scaled output decreases, Control voltage increases to compensate low output. The maximum of $V_{CONTROL}$ is limited to 5.5V and switching stops when $Ct_{(offset)}$ is lower than 0.65V. The pre-converter is compensated to ensure stability over the input voltage and output power range. To compensate the loop, a compensation network is connected between the Control and ground pins.
To ensure high PF, the bandwidth of the loop is set below 20Hz. Compensation network is selected for this design to increase the phase margin.
The compensation network is shown in Figure 21.

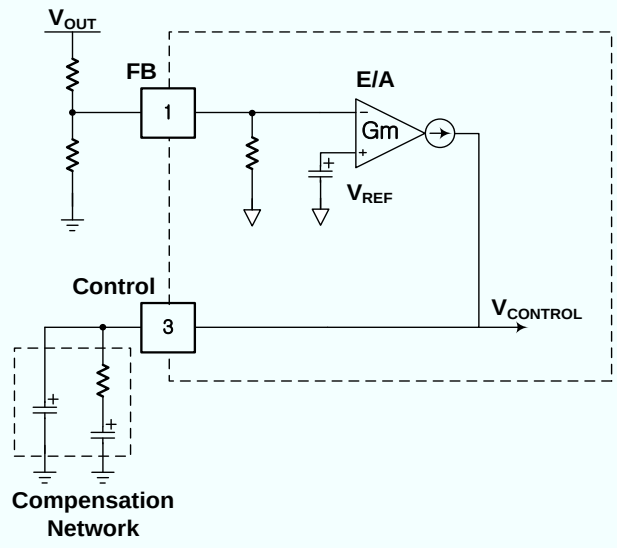


Figure 21. Compensation Network

For the transconductance error amplifier side, gain changes based on differential input. When the error is large, gain is large to make the output dip or peak to suppress quickly. When the error is small, low gain is used to improve power factor performance.

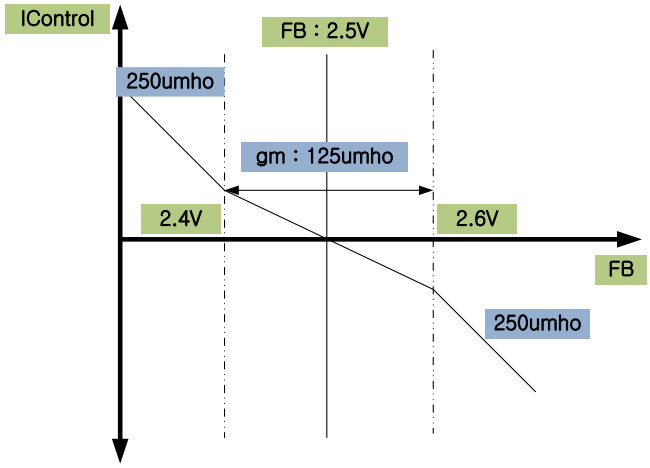


Figure 22. Gain Change

5. Error Amplifier Block

The error amplifier block consists of a OVP comparator, a transconductance amplifier and a UVP comparator. This enables the FB pin to be used for sensing overvoltage or under voltage conditions independently of the error amplifier. The MAP8802B regulates the boost output voltage using an internal error amplifier (E/A). The negative terminal of the EA is pinned out to FB, the positive terminal is connected to a 2.5V±1.6% reference, and the EA output is pinned out to Control. A feature of using a transconductance type amplifier is that the FB pin voltage is only determined by the resistor divider network connected to the output voltage, not the operation of the amplifier. (See Figure21)

6. "Overshoot-less" Startup

Feedback control speed of PFC is quite slow. Due to the slow response, there is a gap between output voltage and feedback control. That is why over-voltage protection (OVP) is critical at the PFC controller and voltage dip caused by fast load changes from light to heavy is diminished by a bulk capacitor. OVP is easily triggered at startup phase. Operation on and off by OVP at startup may cause audible noise and can increase voltage stress at startup, which is normally higher than in normal operation. This operation is better when startup time is very long. However, too long startup time enlarges the output voltage building time at light load. MAP8802B has "overshoot-less" control at startup. During startup, the feedback loop is controlled by an internal proportional gain controller and when the output voltage reaches the rated value, it switches to an external compensator after a transition time. In short, an internal proportional gain controller eliminates overshoot at startup and an external conventional compensator takes over successfully afterward.

7. CS Block

The MOSFET current is sensed using an external sensing resistor for over-current protection. If the CS pin voltage is higher than 0.5V, the over-current protection comparator generates a protection signal. If the boost diode is shorted, the very high current flows through the MOSFET and then the MOSFET is damaged. MAP8802B has a comparator to generate a protection signal if the CS pin voltage is higher than 2.4V. At this time, DRV signal to be off and that is not start operation before VCC is up to UVLO voltage. And to more stable operation of DSP, we are recommend that connect to bid at MOSFET drain current path.

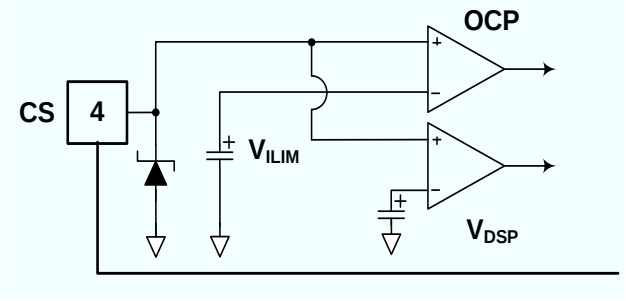


Figure 23. Diode Short Protection

8. ZCD Block

The zero current detector (ZCD) generates the turn-on

signal of the MOSFET when the boost inductor current reaches zero using auxiliary winding coupled to the boost inductor. To activate the ZCD detector of the MAP8802B, the ZCD turns ratio is sized such that at least V_{ZCD} pin during all operating conditions. (See Figure 24) The ZCD pin is protected internally by two clamps, positive clamp voltage is 6.0V and negative clamp voltage is -0.7V. When the auxiliary voltage is higher than 10V, current is sinked through a resistor from the auxiliary winding to the ZCD pin.

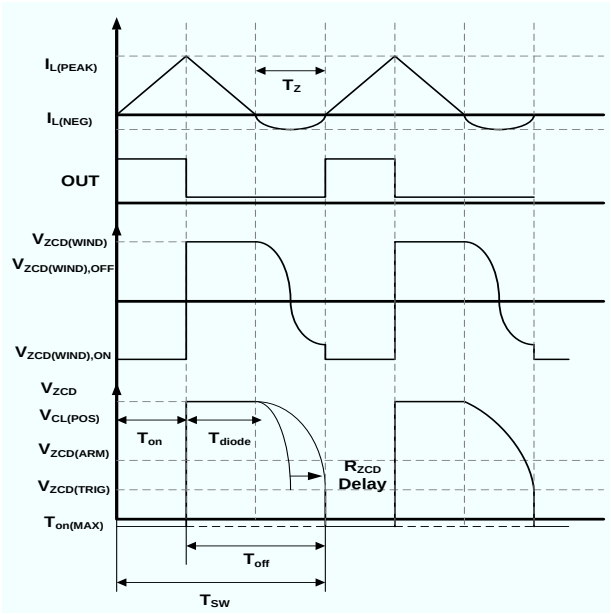


Figure 24. Realistic operation using a ZCD winding

9. Gate output Driver

The MAP8802B includes a powerful output driver capable of sourcing 500mA and sinking 800mA. This enables the controller to drive power MOSFETs efficiently for medium power (≤350W) applications. Additionally, the driver stage provides both passive and active pull down clamps.(Figure 25.) The clamps are active when V_{CC} is off and force the driver output to a voltage less than the turn on threshold voltage of a power MOSFET.

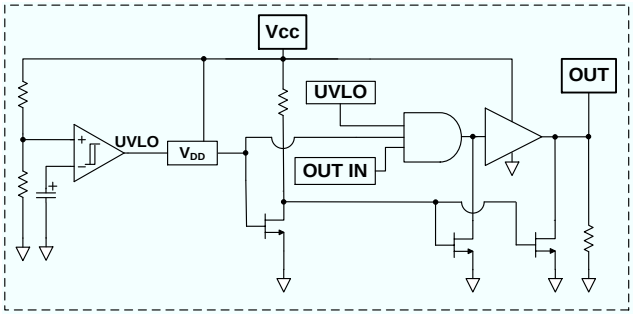


Figure 25. Output Driver Stage and Pull Down Clamps

10. Under-Voltage Protection

When the input voltage is applied to the PFC stage, V_{OUT} is forced to equate to the peak of the line voltage. The MAP8802B detects an under-voltage fault if V_{OUT} is unusually low, such that V_{FB} is less than V_{UVP}. During an UVP fault, the drive and error amplifier are disabled.

The UVP feature protects the application if there is a disconnection in the power path to C_{BULK} or if R_{OUT1} is disconnected.

11. Over-Voltage Protection

The low bandwidth of the feedback network causes active PFC stages to react to changes in output load or input voltages slowly. Consequently, there is a risk of overshoots during transient conditions. It is critical that overvoltage protection (OVP) prevents the output voltage from exceeding the ratings of the PFC stage components. The MAP8802B detects excessive V_{OUT} voltage and disables the driver until V_{OUT} decreases. OVP ensures that Vout is within the PFC stage component ratings.

A comparator connected to the FB pin provides the OVP protection.

12. ZCD Short Protection

Max Frequency Limit

This function prevents the operation of the CCM and the burning of wires when the Aux short,(See Figure 26) The initial operation starts with CCM mode because the output voltage is lower than input. The CCM operation let the switching frequency increase until output voltage approaches the setting voltage. At this moment, the frequency is over 2MHz. MAP8802B is designed to be operated in critical conduction mode (CRM). However, when Aux short occurs, IC cannot operate with CRM mode because the ZCD voltage cannot be detected. At this moment, the operation mode is CCM and frequency is over 2MHz. Therefore, maximum frequency limit is required because the high frequency is occurred the burning of wire.

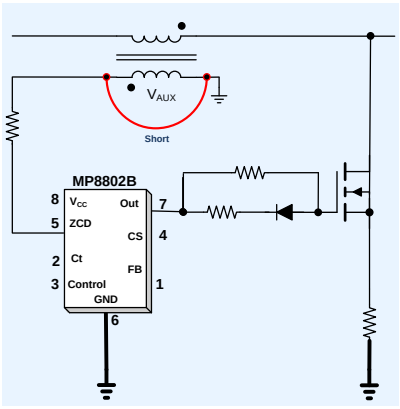


Figure 26. Aux wire short

Off timer protection

If ZCD noise is not existed, MAP8802B is operating as off timer (T-start timer) because ZCD signal is be absent.

But It is can be occurred audible noise because the period is about 150us.(about 6Khz) To prevent audible noise, MAP8802B detects the cycle of Tstart Timer. If Tstart Timer reached 16cycle, MAP8802B entered Auto-restart protection mode.

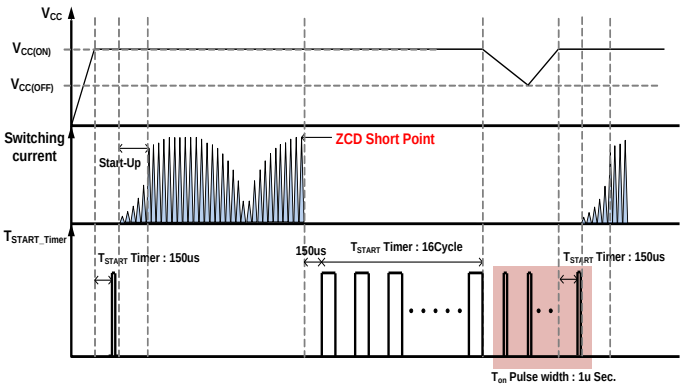


Figure 27. ZCD off timer protection

Typical Application Circuit

1. Demonstration board specification.

The electronic design tool allows the user to easily determine most of the system parameters of a boost pre−converter. The demonstration board accepts a universal ac line-input voltage (85Vac~265Vac), and produces an output voltage of 400Vdc for loads up to 0.5A (PO = 200W).In demonstration board, the bypass diode (DP102) & RC resistor of CS block filter is optional. The detail demonstration design information described in our Application note.

2. Operating information.

INPUT Range	Output Power	Output Voltage
85Vac ~ 265Vac	200W	400V(0.5A)

3. Transformer information.

3.1 Winding specification

	PIN	WIRE	TURNS
Np	4,5 → 2,3	0.1φ*60	49
Insulation Tape		0.05mm	3
Naux	7 → 9	0.5φ*1	6
Insulation Tape		0.05mm	3

3.2 Inductance & Core

	Pin	Spec.	Remark
Inductance	3,4 → 1,2	200μH ± 5%	100kHz, 1V
CORE	-	EER3124	SAMHWA(PL-7)

4. Application Schematic

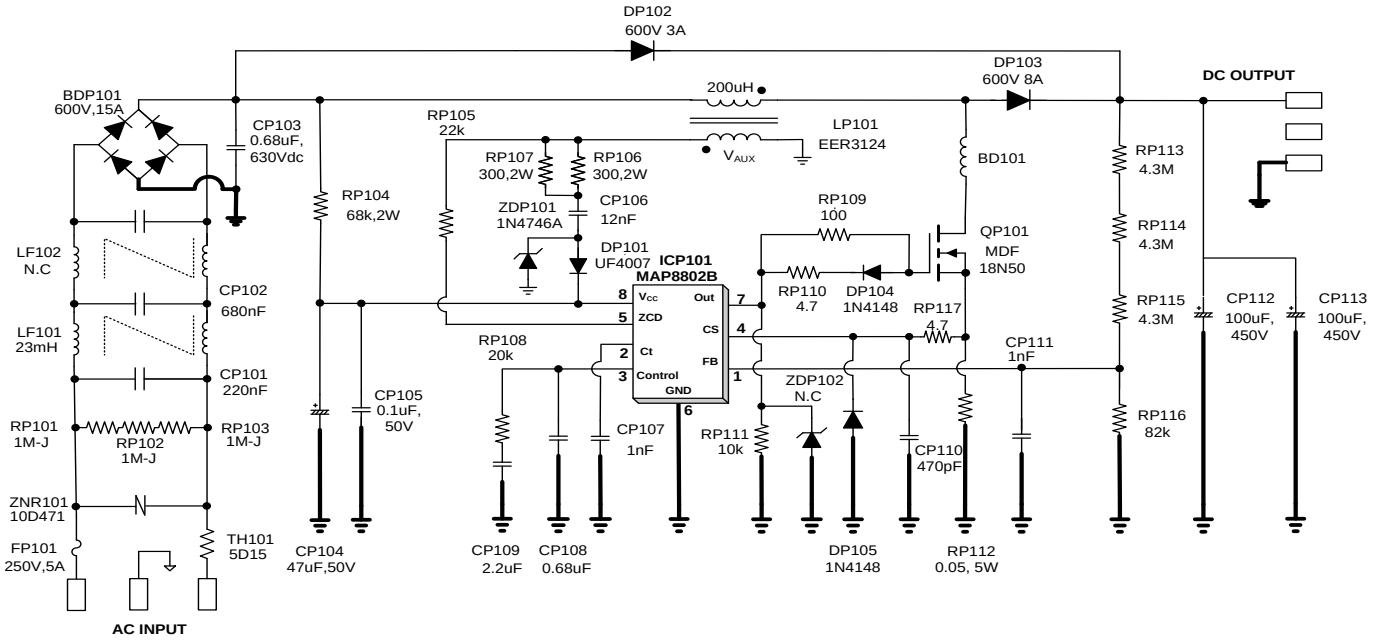


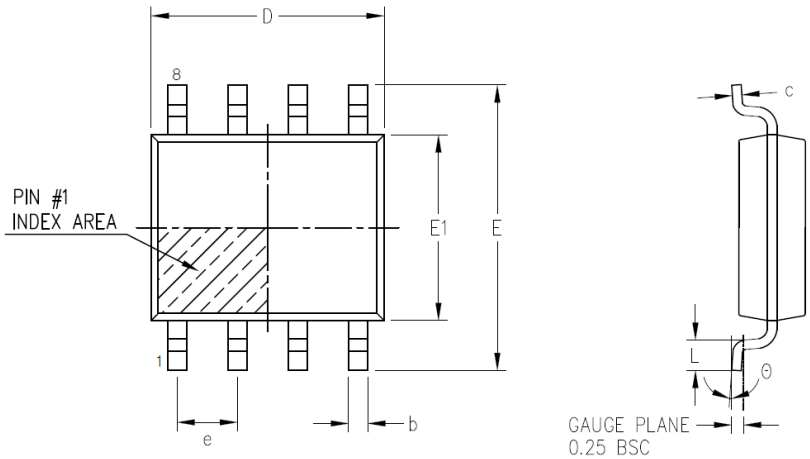
Figure 28. Application Schematic

BOM List

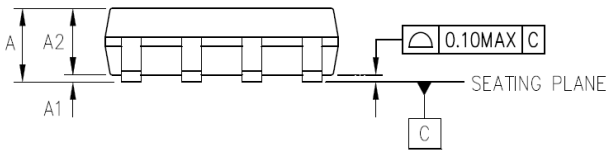
MAP8802B 200W Wide-Range Application Circuit Components List

Part	Value	Note	Part	Value	Note
IC			**MOSFET**		
ICP101	MAP8802B	MagnaChip (8-SOP)	QP102	MDF18N50	MagnaChip (TO-220)
NTC			**Zener Diode**		
TH101	5D-15		ZDP101 ZDP102 ZDP103	1N4746 N.C 1N4746	Fairchild
Resistor			**Capacitor**		
RP101 RP102 RP103	1M-J	1/8W (SMD-2012)	CP101	220nF/275Vac	X - Capacitor
RP104	68K-J	2W	CP102	680nF/275Vac	X - Capacitor
RP105	22K-J	1/4W (SMD3216)	CP103	680nF/630Vdc	Box capacitor
RP106 RP107	300-J	2W	CP104	47uF /50V	Electrolytic Capacitor
RP108	20K-J	1/8W (SMD-2012)	CP105	0.1uF/50V	Chip Capacitor
RP109	47-J	1/8W (SMD-2012)	CP106	12nF/50V	Film Capacitor
RP110	4.7-J	1/8W (SMD-2012)	CP107	1nF/50V	Chip Capacitor
RP111	10K-J	1/8W (SMD-2012)	CP108	0.68uF/16V	Chip Capacitor
RP112	0.05-J	5W	CP109	2.2uF/16V	Chip Capacitor
RP113 RP114 RP115	4.3M-F	1/8W (SMD-2012)	CP110	470pF/50V	Chip Capacitor
RP116	82K-F	1/8W (SMD-2012)	CP111	1nF/50V	Chip Capacitor
RP117	10-J	1/8W (SMD-2012)	CP112 CP113	120uF/450V	Electrolytic Capacitor
Fuse					
FP101	5.0AL/250V		**Diode**		
Varistor			DP101	UF4007(1000V 1A)	VISHAY
ZNR101	10D - 471	470V	DP102	UF5408(1000V 3A)	VISHAY
Line Filter			DP103	FSU10B60	Nihon Inter
LF101 LF102	23mH N.C	Wire0.7mm	DP104 DP105	MMBD4148	Fairchild
Bridge Diode			**Inductor**		
BDP101	GBJ1506	DIODE	LP101	200uH	EER3124
Connector					
CN101 CN102	YHW396-03V				

Physical Dimensions



Symbol	Dimension (mm)		
	Min	Nom	Max
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	–	1.27
Θ	0°	–	8°



NOTES :

1. Reference JEDEC MS-012(AA)
2. Package length and width do not include mold flash, protrusions or gate burrs.
3. The configuration of PIN #1 identifier/chamfer feature is optional

DISCLAIMER:

The products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.