MAP3621

1-CH Average Current Control Buck Controller for LED Backlight

General Description

MAP3621 is a single channel average-mode current control buck controller for LED backlight application. It does not require an additional dimming MOSFET and utilizes constant off-time control and average current control feedback without external loop compensation or high-side current sensing.

MAP3621 features ±1% CS voltage accuracy and has dedicated Independent analog dimming input up to 3.3V. It can be powered from 8.5V ~ 18V supply.

MAP3621 provides MOSFET DS short (FLT output), sense resistor short protection, SCP and UVLO.

MAP3621 is available 14 leads SOIC with Halogen-free (fully RoHS compliant).

RoHS Compliant
HALOGEN-FREE

Features

- 8.5V to 18V Input Voltage Range
- Average-Mode Current Control
- Mixed Programmable Constant Off-time
- Up to 3.3V Analog Dimming
- ±1% CS Voltage Accuracy
- Direct PWM Dimming Input
- Fault Output
  - MOSFET Drain-Source Short
- Short Circuit Protection
- Sense Resistor Short Protection
- UVLO
- 14 Leads SOIC Package with Halogen-free

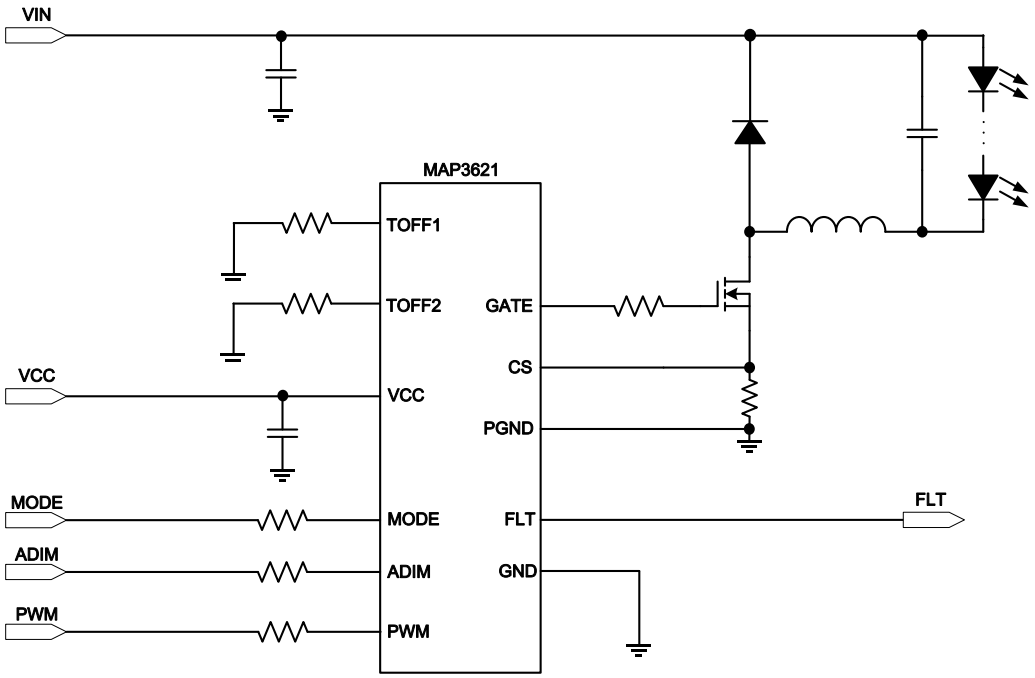
Applications

- High Brightness white LED backlighting for LCD TVs
- General LED lighting applications

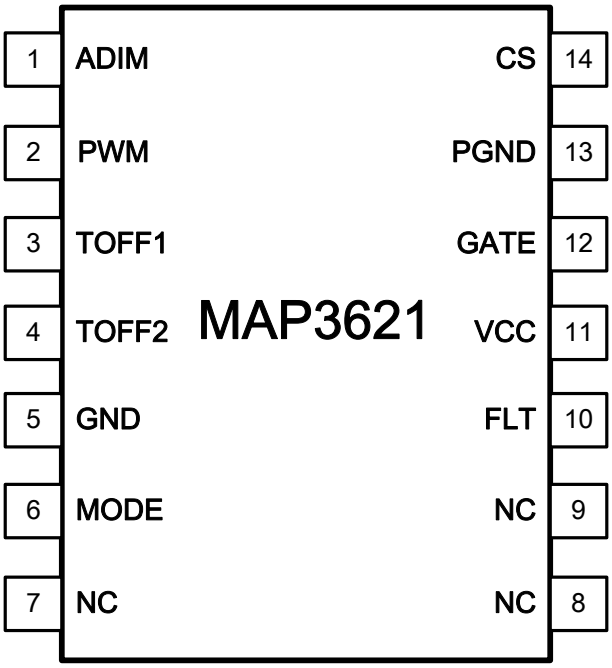
Ordering Information

Part Number	Top Marking	Ambient Temperature Range	Package	RoHS Status
MAP3621SIRH	MAP3621	-40℃ to +85℃	14Leads SOIC	Halogen Free

Typical Application



Pin Configuration



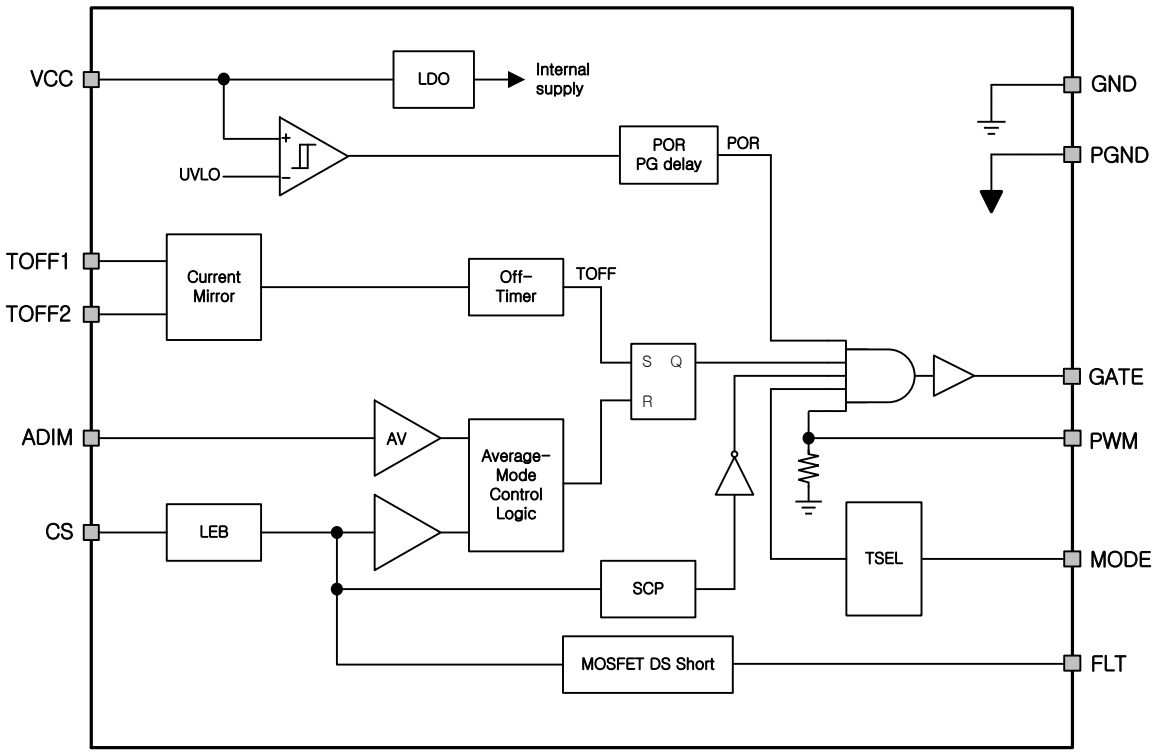
SOIC-14L

Pin Description

14leads SOIC	Name	Description
1	ADIM	Setting for CH LED current thru external DC voltage
2	PWM	PWM signal input for CH
3	TOFF1	Setting for normal switching off-time (Note 1)
4	TOFF2	Setting for initial switching off-time (Note 1)
5	GND	Signal Ground
6	MODE	Setting for duration time that initial switching off-time(TOFF2)
10	FLT	Fault Output
11	VCC	Power supply input. Need external bypass capacitor.
12	GATE	GATE driver output to drive external NMOSFET for CH
13	PGND	Power GND for CH
14	CS	External current sense for CH(Note 2)
7, 8, 9	NC	No connection (Note 3)

Note 1: Connect external resistor to GND to set Switching off-time as shown in typical application
Note 2: Connect external resistor to PGND to sense the external power MOSFET source current as shown in typical application
Note 3: Must be connected to GND externally.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Min	Max	Unit
V_{VCC}, V_{GATE}, V_{PWM}, V_{MODE}	VCC, GATE, PWM, MODE pins Voltage	-0.3	20	V
V_{CS}, $V_{TOFF1/2,}$ V_{ADIM}, V_{FLT}	CS, TOFF1/2, ADIM, FLT pins Voltage	-0.3	5.5	V
T_{PAD}	Soldering Lead/ Pad Temperature 10sec		300	°C
T_J	Junction Temperature	-40	+150	°C
T_S	Storage Temperature	-65	+150	°C
ESD	HBM on All Pins (Note 2)	-2000	+2000	V
	MM on All Pins (Note 3)	-200	+200	
	CDM on All Pins (Note 4)	-500	+500	

Note 1: Stresses beyond the above listed maximum ratings may damage the device permanently. Operating above the recommended conditions for extended time may stress the device and affect device reliability. Also the device may not operate normally above the recommended operating conditions. These are stress ratings only.
Note 2: ESD tested per JESD22A-114.
Note 3: ESD tested per JESD22A-115.
Note 4: ESD tested per JESD22C-101

Recommended Operating Conditions (Note 1)

Parameter		Min	Max	Unit
V_{Vcc}	Supply Input Voltage	8.5	18.0	V
V_{ADIM}	ADIM Input Range	0.0	3.3	V
T_A	Ambient Temperature (Note 2)	-40	+85	°C

Note 1: Normal operation of the device is not guaranteed if operating the device over outside range of recommended conditions.
Note 2: The ambient temperature may have to be derated if used in high power dissipation and poor thermal resistance conditions.

Package Thermal Resistance (Note 1)

Parameter		θJA	θJC	Unit
MAP3621SIRH	14 Leads SOIC	76.3	36.5	℃/W

Note 1: Multi-layer PCB based on JEDEC standard (JESD51-7)

Electrical Characteristics

Unless noted, V_{VCC} = 12V, C_{VCC} = 1.0μF, and typical values are tested at T_A = 25°C.

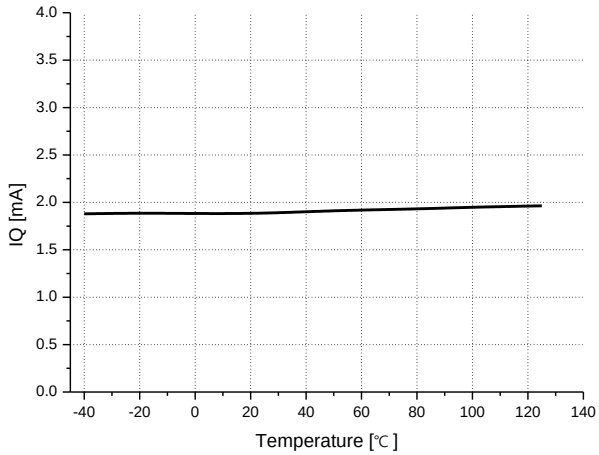
Parameter		Test Condition	Min	Typ	Max	Unit
Supply						
V_{VCC}	Input Voltage Range		8.5		18	V
I_Q	Quiescent Current	V_{PWM} = 5V, V_{CS} = 0V		2		mA
V_{UVLO}	Under Voltage Lockout Threshold Voltage on VCC pin	Release threshold(rising V_{VCC})	7.5	8.0	8.5	V
		Lockout hysteresis(falling V_{VCC})	0.5	1.0	1.5	
t_{PG_DELAY}	Power Good Delay Time			500		ms
OFF Timer						
t_{OFF1}	Switching Off-time1	R_{TOFF1}=50kΩ	4.5	5.0	5.5	us
		R_{TOFF1}=103kΩ	9	10	11	
t_{OFF2}	Switching Off-time2	R_{TOFF2}=36kΩ		1.0		us
t_{MODE}	t_{OFF2} duration time	V_{MODE} = 1V		112		us
		V_{MODE} = 3V		308		
t_{ON_MAX}	Max. On-Time			37		us
t_{OFF_MIN}	Min. Off-Time			1.2	1.5	us
D_{MAX}	Max. Duty Cycle (Note 1)	V_{ADIM} = 3.3V, t_{OFF}=1.2us		97		%
Current Sense & Dimming						
V_{ADIM}	ADIM Input Voltage Range		0.0		3.3	V
A_V	VADIM to CS Voltage Ratio		0.5*(0.66+0.3*VADIM)			V/V
V_{CS}	CS Voltage	V_{ADIM} = 0.0V	0.3267		0.3333	V
		V_{ADIM} = 3.3V	0.8167		0.8333	
t_{LEB}	Leading Edge Blanking Time	(Note 1)		300		ns
Logic Interface						
V_{PWM}	Logic Input Level on PWM pins	V_{PWM_L} : Logic Low			0.8	V
		V_{PWM_H} : Logic High	2.0			
R_{PWM}	Pull-down Resistor on PWM pins	V_{PWM} = 4V	50	100	150	kΩ
V_{MODE}	Low Level on MODE pin			0.7		V
GATE Driver						
I_{SOURCE}	GATE Source Current	V_{GATE} = 0V,		300		mA
I_{SINK}	GATE Sink Current	V_{GATE} = V_{VCC}=12V		600		mA
t_{RISE}	GATE Output Rising Time	C_{GATE}=1nF, V_{VCC} = 12V		70	150	ns
t_{FALL}	GATE Output Falling Time	C_{GATE}=1nF, V_{VCC} = 12V		35	100	ns
Protection						
V_{SCP}	SCP Detection Threshold Voltage on CS pins		2.375	2.500	2.625	V
t_{DELAY}	SCP Delay Time			300		ns
$t_{RESTART}$	Restart Time			1		ms
V_{CSP}	RCS Short Detection Threshold Voltage on CS pin		0.15	0.20	0.25	V
t_{CSP}	RCS Short Detection Time			30		us
V_{SCPDS}	MOSFET DS Short Detection Threshold Voltage on CS pin	V_{PWM_H} : Logic High	2.375	2.500	2.625	V
		V_{PWM_L} : Logic Low	0.65	0.70	0.75	
t_{SCPDS}	MOSFET DS Short Detection Time			30		us
V_{FLT}	FLT pin High Voltage		4.5		5.5	V
R_{FLT}	FLT pin Internal Resistance	I_{FLT}=100uA	500	1000	1500	Ω

Note 1: These parameters, although guaranteed by design, are not tested in mass production.

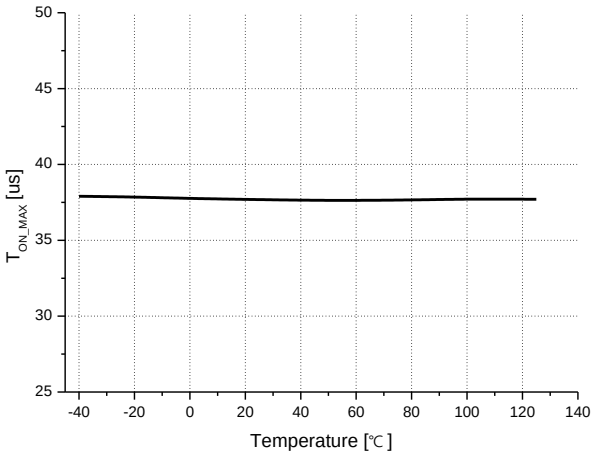
Typical Operating Characteristics

Unless otherwise noted, V_{VCC} = 12V and T_A = 25°C.

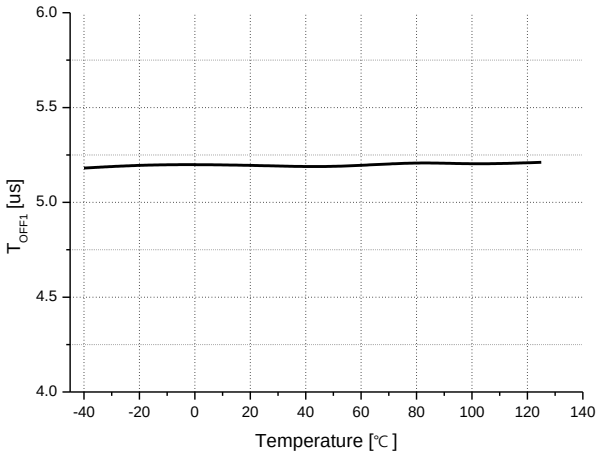
Quiescent Current vs. Temp



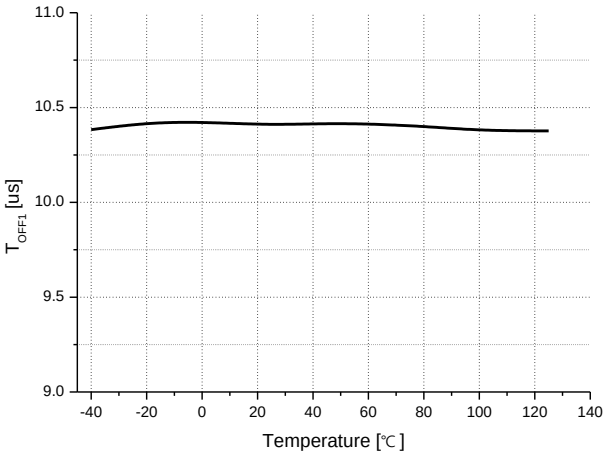
GATE MAX ON TIME vs. Temp.



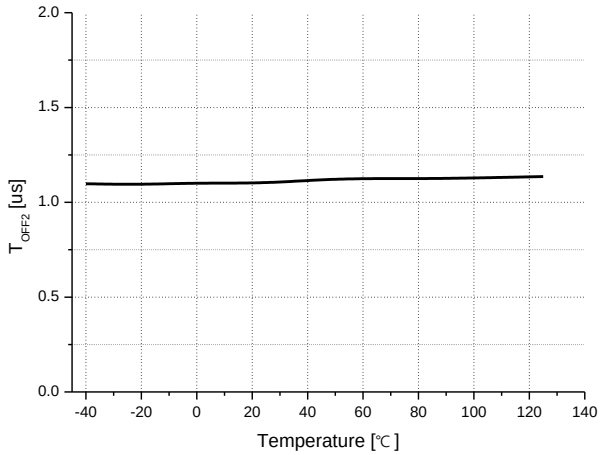
t_{OFF}(R_{TOFF}=50kΩ) vs. Temp.



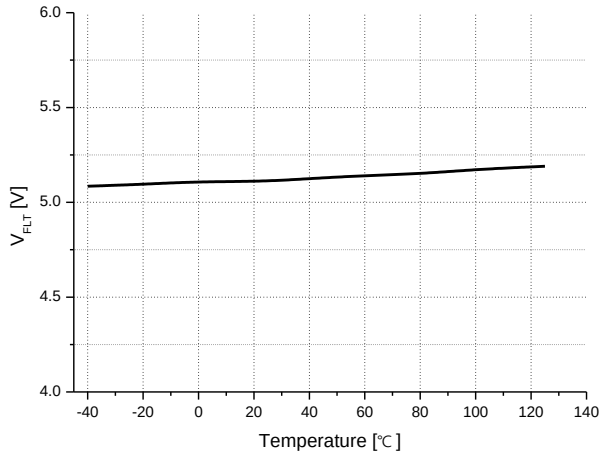
t_{OFF}(R_{TOFF}=103kΩ) vs. Temp.



t_{OFF2}(R_{TOFF}=36kΩ) vs. Temp.



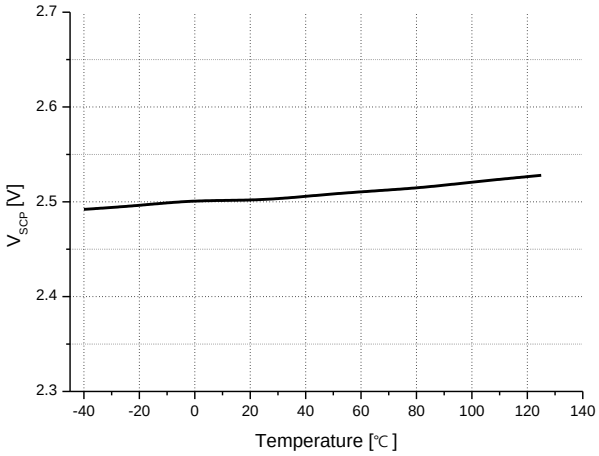
V_{FLT} vs. Temp.



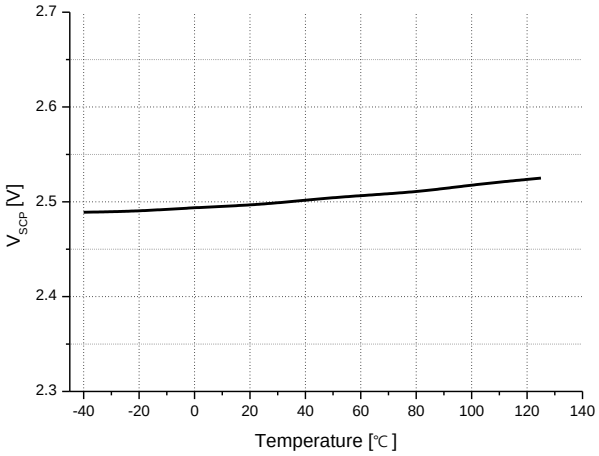
Typical Operating Characteristics

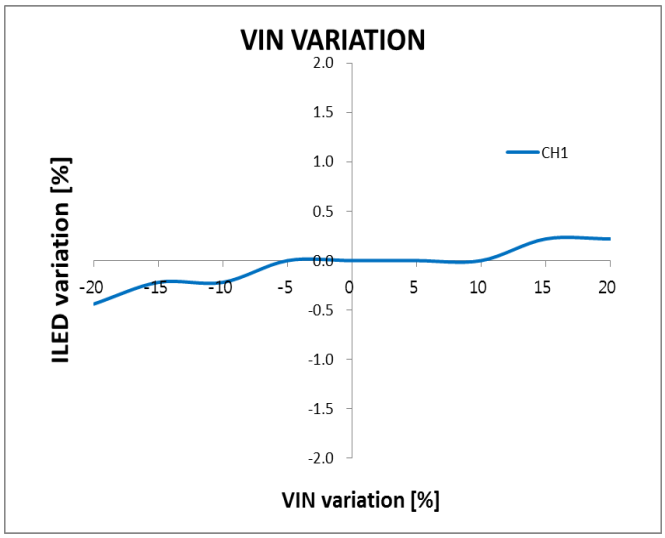
Unless otherwise noted, V_{VCC} = 12V and T_A = 25°C.

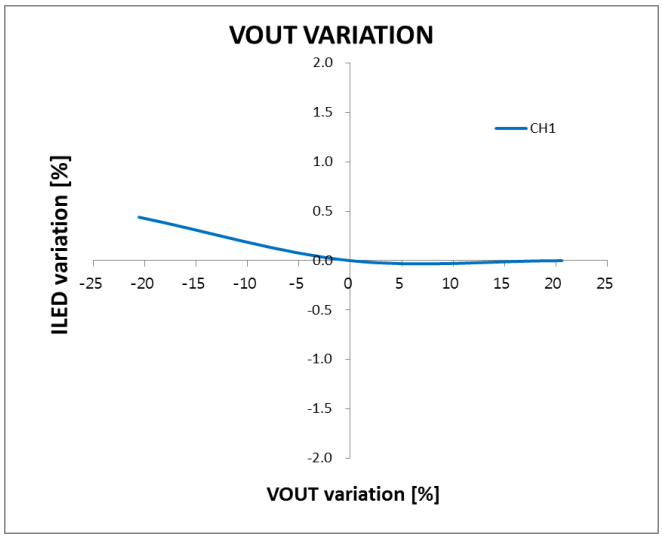
V_{SCP} vs. Temp.

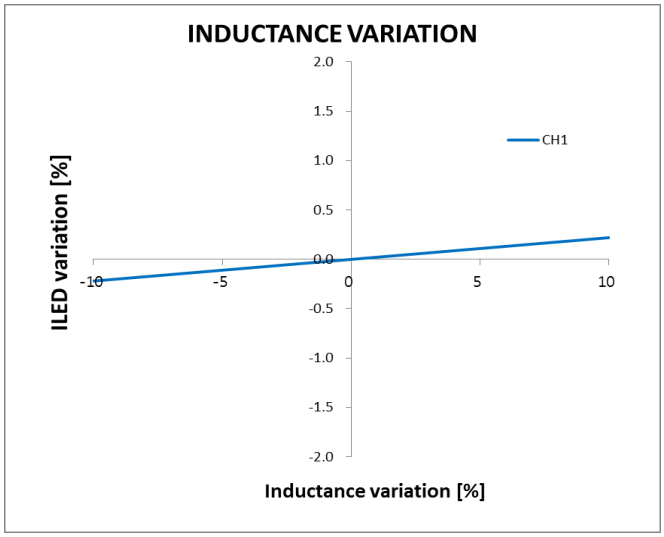


V_{SCP_DS} vs. Temp









Functional Description

GENERAL DESCRIPTION

The MAP3621 is single channel low-side single switch control, constant off-time buck controller optimized to LED backlight applications. The IC employs unique average-mode current control architecture which provides precise LED current accuracy. It does not require any external loop compensation or high side current sensing.

The IC operates at continuous conduction mode to reduce output ripple, thus small output capacitor is available. The off-time is user adjustable through the selection of an external resistor, this allows the design to be optimized for a given switching frequency range and supports wide range of input voltages.

GATE TOFF OPERATION and SETTING

The off-time of the GATE driver is programmed by an external resistor connected between the TOFF pin and ground. Do not leave this pin open.

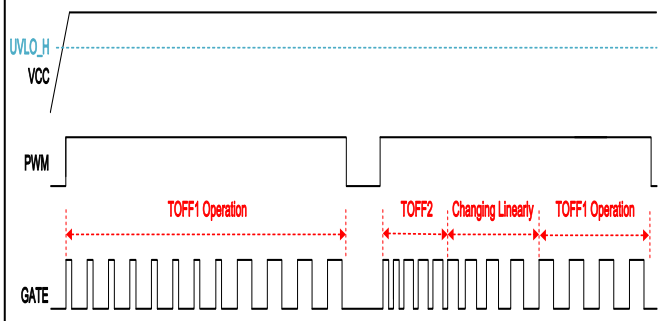
The MAP3621 operates by changing the off time of the GATE in the PWM on Duration time.

If the output cap was discharged during the initial start-up, high-speed switching may cause LED current overshoot. So, in the first PWM on after UVLO_H, it operates with normal frequency TOFF1.

At second PWM on, it operates at GATE off time by TOFF2 and TOFF2 operation hold time is determined by MODE voltage. When TOFF2 operation is completed, TOFF1 changes to GATE OFF time. At this time, sudden change of frequency causes LED current dip. The MAP3621 improves the LED current dip phenomenon by changing the gate off time linearly for a certain period of time (70us) after the TOFF2 operation is completed.

When the MODE voltage is 1V, the TOFF2 operates for 112us, and at 3V it operates for 308us.

When the MODE voltage is VCC level, the function is not used and only operates with TOFF1.



The off-time is calculated by following equation.

$$TOFF1 = \frac{(RTOFF1 + 1.6104)}{10.401}[us]$$

$$TOFF2 = \frac{(RTOFF2 + 5.439)}{41.308}[us]$$

MAX. ON-TIME

The max. on-time of Switching is limited 37us.

Care should be taken to choose input voltage which should not exceed this on-time limit(especially OD mode).

The on-time of Switch can be calculated by following equations.

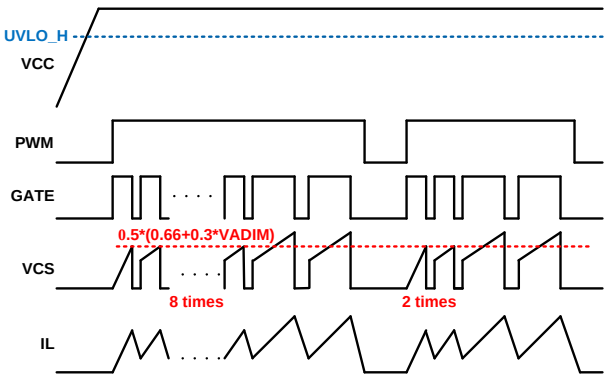
$$D = \frac{V_{LED}}{V_{IN}}$$

$$t_{ON} = \frac{D \times t_{OFF}}{1 - D}$$

Finally, $t_{ON} < t_{ON\_MAX\ Value}$

SOFT-START

The MAP3621 operates at peak current mode at initial start-up and every rising edge of PWM input to smooth inductor current ramp-up(output capacitor charging phase). The number of peak-controlled switch cycles is 8 times at initial start-up and 2 times at every PWM rising edge as following figure.



LED CURRENT

The LED current is calculated by following equation.

$$ILED = \frac{0.5 * (0.66 + 0.3 * VADIM)}{RCS} [A]$$

The ADIM voltage range is from 0.0V to 3.3V.
In terms of total system accuracy of LED current, the larger inductance and the slower switching frequency, the better accuracy.

FLT OUTPUT

If any of following events occurs, the FLT pin goes to logic HIGH state immediately. The protection status is latched and can be cleared by applying a complete power-on-reset(POR).

MOSFET Drain-Source Short

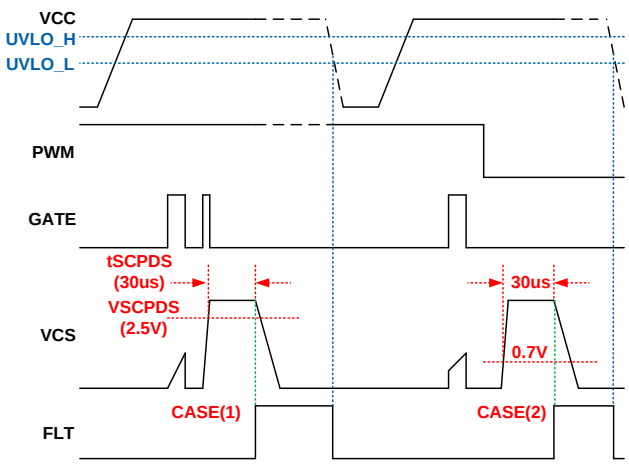
MOSFET DRAIN-SOURCE SHORT DETECTION

The CS voltage depends on input voltage(VIN) and sense resistor(RCS) value at short status between drain and source of MOFSET.
In case the following drain-source short events of internal MOSFET occur, the FLT pin goes to logic HIGH state immediately.

CASE(1) - At dimming(PWM=logic HIGH):
At first, SCP will be happened. Even though the Switch is off-state by SCP, if the CS voltage exceeds typ. 2.5V for more than 30us.

CASE(2) - At PMW Logic LOW:
Even though the Switch is off-state, if the CS voltage exceeds typ. 0.7V for more than 30us.

Following timing charts show this operation.

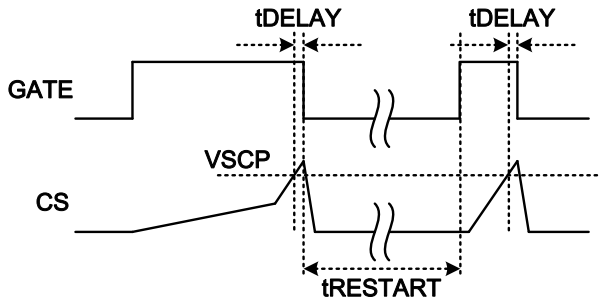


UVLO

The MAP3621 has an Internal LDO regulator to supply internal circuit. This LDO is powered up when the VCC voltage rises to UVLO release threshold.
If the voltage on the VCC pin falls below UVLO lockout threshold, the device turns-off the Switching and be reset. This ensures fail-safe operation for VCC input voltage falling.

SCP

If the CS voltage rises V_{SCP} during normal operation, the MAP3621 turns-off the Switch after t_{DELAY}(typ. 300ns) time. The auto-restart time is typ. 1ms($t_{RESTART}$). This protects for hard instantaneous short such as catch diode, inductor or LED bar short.



RCS SHORT PROTECTION

If the CS pin is shorted to GND due to current sense resistor(R_{CS}) short, there is a potential danger of the over-current condition not being detected. The MAP3621 can protect this short event.
If the CS pin voltage is equal or lower than typ. 0.2V(V_{CSP}) for more than typ. 30us(t_{CSP}), the IC turns off the Swtich immediately.

Inductor

In order to achieve accurate constant current output, the MAP3621 is required to operate in Continuous Conduction Mode (CCM) under all operating conditions. In general, the magnitude of the inductor ripple current should be kept as small as possible. If the PCB size is not limited, higher inductance values result in better accuracy of the output current. However, in order to minimize the physical size of the circuit, an inductor with minimum physical outline should be selected such that the converter always operates in CCM and the peak inductor current does not exceed the saturation current limit of the inductor.

The Min. inductance (boundary inductance) which guarantees CCM operation can be calculated as;

$$\Delta I_{LB} = 2I_{OUT}$$

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{LB}} \times t_{OFF} = \frac{V_{OUT} \times (1-D)}{2 \times I_{OUT} \times f_{SW}}$$

The ripple current through chosen inductor is as following equation;

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

For example, in case V_{IN}=175V, V_{OUT}=135V, I_{OUT}(I_{LED})=425mA, f_{SW}=50kHz and target ripple current=300mA;

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{135}{175} = 0.77$$

$$L_{MIN} = \frac{V_{OUT} \times (1-D)}{2 \times I_{OUT} \times f_{SW}} = \frac{135 \times (1-0.77)}{2 \times 0.425 \times 50 \times 10^3} = 0.73[mH]$$

The ripple current at L_{MIN} is 2*I_{OUT}=850[mA] and this is too large to use.

For target ripple current(ΔI_L=300mA);

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}} = \frac{(175-135) \times 0.77}{0.3 \times 50 \times 10^3} = 2.05[mH]$$

In this case, the chosen conventional inductor is 2mH/1A.

Freewheeling Diode

The freewheeling diode is chosen based on its maximum stress voltage, its maximum peak current and total power losses. The power losses are lower for a larger duty cycle and vice-versa, because the diode is opened (connected) during off-time.

Maximum voltage stress across the diode is equal to the input voltage V_{IN}, and therefore the power diode must be selected with some voltage margin. For example, if the input voltage is maximally 400 V, then maximum repetitive peak reverse voltage (V_{RRM}) should be 450 V or higher.

Maximum peak diode current is selected in order to calculate the inductor size. Also in this case, the catch diode must be selected with some current margin.

The voltage drop across the diode in a conducting state is primarily responsible for the losses in the diode. The power dissipated by the diode can be calculated as the product of the forward voltage and the output load current for the time that the diode is conducting. The switching losses which occur at the transitions from conducting to non-conducting states are very small compared to conduction losses and are usually ignored. The power dissipated by the catch diode is given by:

$$P_D = V_D \times I_O \times (1-D)$$

Where, V_D is the forward voltage drop of the freewheeling diode.

Input Capacitor

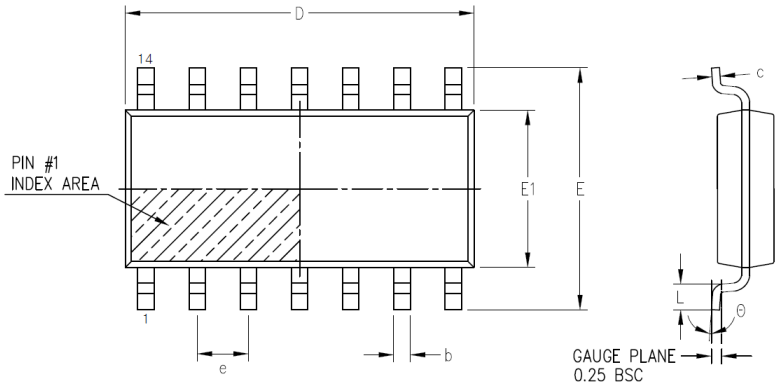
Select the input capacitor to ensure that the input voltage ripple is within a desired range (1% to 5% of the input bus voltage). The input capacitor is usually electrolytic and its ESR dominates its impedance.

A 4.7μF to 22μF electrolytic capacitor will usually suffice.

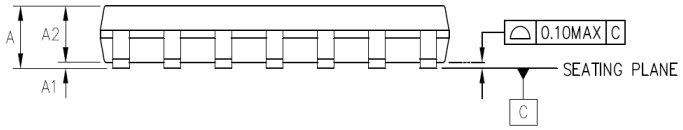
Output Capacitor

Selecting a suitable capacitor can reduce LED current ripple and increase LED life-time. Note that having too large of a capacitance will cause the LED current to respond slowly. The typical value of the capacitor is 0.33μF.

Physical Dimensions



Symbol	Dimension (mm)		
	Min	Nom	Max
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	–	1.27
θ	0°	–	8°



NOTES :

1. Reference JEDEC MS-012(AB)
2. Package length and width do not include mold flash, protrusions or gate burrs.
3. The configuration of PIN #1 identifier/chamfer feature is optional

14 **Leads SOIC**