



AMDUA040N070RH

Dual N-channel Trench MOSFET 40V 7.0mΩ 35A

FEATURES

- Trench power MOSFET technology
- N-channel, normal level
- 100% Avalanche tested
- Maximum 175°C junction temperature
- AEC-Q101 qualified

APPLICATIONS

- Motor inverter
- Switching applications

KEY PERFORMANCE PARAMETERS

V_{DS}	40	V
$R_{DS(on), typ.}$	0.0061	Ω
I_D	35	A
Q_g	24	nC
Junction temperature, max	175	°C

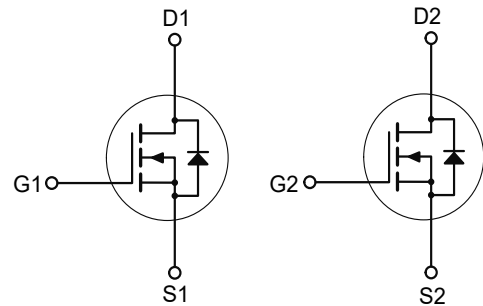


Top View

PDFN56-DUAL



Bottom View



RoHS Compliant
HALOGEN-FREE

ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
AMDUA040N070RH	PDFN56-DUAL	040N070	Tape & Reel	Halogen Free

<http://www.magnachip.com/>

ABSOLUTE MAXIMUM RATINGS, at $T_c = 25^{\circ}\text{C}$, unless otherwise specified

PARAMETER		SYMBOL	RATING	UNIT
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	
Drain current	$T_c=25^{\circ}\text{C}$ (Silicon Limited)	I_D	70	A
	$T_c=25^{\circ}\text{C}$ (Package Limited)		35	
	$T_c=100^{\circ}\text{C}$ (Silicon Limited)		49	
	$T_c=100^{\circ}\text{C}$ (Package Limited)		35	
¹⁾ Pulsed drain current	$T_c=25^{\circ}\text{C}$	I_{DM}	140	
Total power dissipation	$T_c=25^{\circ}\text{C}$	P_{tot}	60	W
	$T_c=100^{\circ}\text{C}$		30	
²⁾ Avalanche energy, single pulse		E_{AS}	45	mJ
Operating and storage temperature		T_J, T_{stg}	- 55 ~ 175	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATING	UNIT
Thermal resistance, junction - case	$R_{\theta JC}$	2.5	$^{\circ}\text{C/W}$
³⁾ Thermal resistance, junction - ambient	$R_{\theta JA}$	50	

ELECTRICAL CHARACTERISTICS (T_J = 25°C)**STATIC CHARACTERISTICS**

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Drain-source breakdown voltage	V _{(BR)DSS}	40	-	-	V	V _{GS} =0 V, I _D =250 μA
Gate threshold voltage	V _{GS(th)}	2.45	3.20	3.95	V	V _{DS} =V _{GS} , I _D =250 μA
Zero gate voltage drain current	I _{DSS}	-	-	1	μA	V _{DS} =40 V, V _{GS} =0 V
Gate-source leakage current	I _{GSS}	-	-	± 100	nA	V _{GS} =±20 V, V _{DS} =0 V
Drain-source on-state resistance	R _{DS(on)}	-	6.1	7.0	mΩ	V _{GS} =10 V, I _D =17.5 A
⁴⁾ Gate resistance	R _G	-	2.3	-	Ω	f=1 MHz
⁴⁾ Transconductance	g _{fs}	-	42	-	S	V _{DS} =10 V, I _D =17.5 A

⁴⁾ DYNAMIC CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Input capacitance	C _{iss}	-	1658	2321	pF	V _{GS} =0 V, V _{DS} =20 V, f=1 MHz
Output capacitance	C _{oss}	-	445	623		
Reverse transfer capacitance	C _{rss}	-	41	66		
Turn-on delay time	t _{d(on)}	-	17	-	ns	V _{DD} =20 V, V _{GS} =10 V, I _D =17.5 A, R _{G,ext} =3 Ω
Rise time	t _r	-	11	-		
Turn-off delay time	t _{d(off)}	-	27	-		
Fall time	t _f	-	9	-		

⁴⁾ GATE CHARGE CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Gate to source charge	Q _{gs}	-	9	13	nC	V _{DD} =20 V, I _D =17.5 A, V _{GS} =0 to 10 V
Gate charge at threshold	Q _{gs(th)}	-	5	-		
Gate to drain charge	Q _{gd}	-	3	5		
Switching charge	Q _{sw}	-	7	-		
Gate charge total	Q _g	-	24	34		
Gate plateau voltage	V _{plateau}	-	5.1	-	V	

SOURCE-DRAIN DIODE

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
⁴⁾ Diode continuous forward current	I _S	-	-	35	A	-
⁴⁾ Diode pulse current	I _{S,pulse}	-	-	140	A	pulsed; t _p ≤ 10 μs
Diode forward voltage	V _{SD}	-	0.9	1.2	V	V _{GS} =0 V, I _F =17.5 A
⁴⁾ Reverse recovery time	t _{rr}	-	35.9	-	ns	I _F =17.5 A, di _F /dt=100 A/μs
⁴⁾ Reverse recovery charge	Q _{rr}	-	19.4	-	nC	

Notes

1. Pulse width limited by T_{Jmax}
2. Starting T_J=25°C, L=1mH, I_{AS}=9.5A, V_{DD}=36V, V_{GS}=10V
3. Surface mounted FR-4 board by JEDEC (jesd51-7)
4. The parameter is not subject to production testing - guaranteed by design.

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 °C, unless otherwise noted)

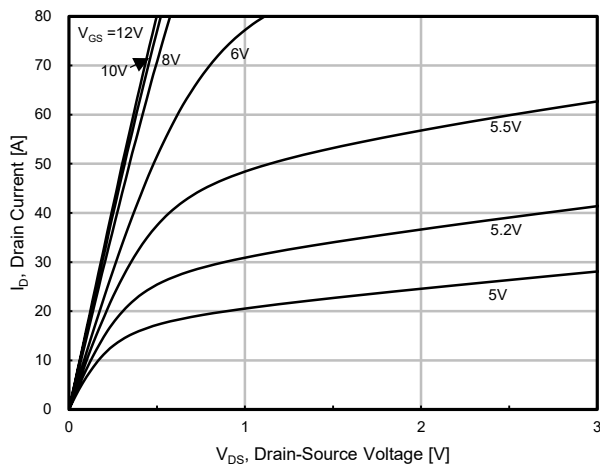


Fig. 1. Output Characteristics (25°C)

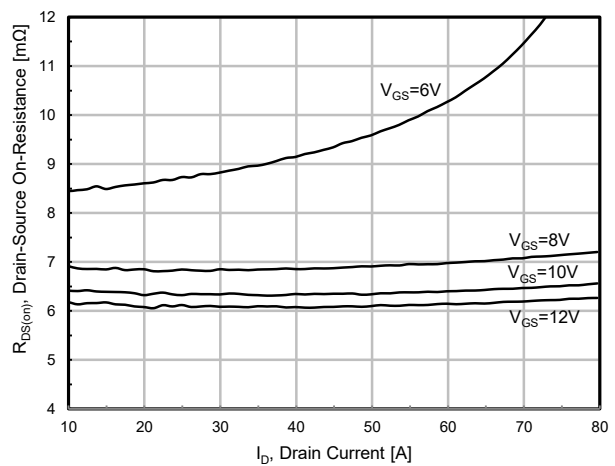


Fig. 2. Static On-Resistance Variation

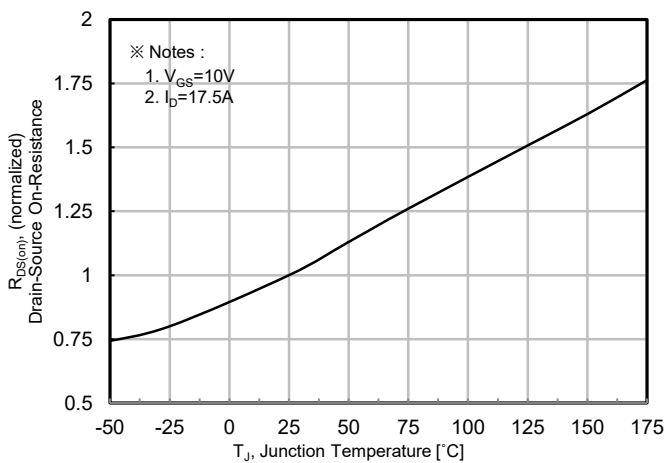


Fig. 3. On-Resistance vs. Junction Temperature

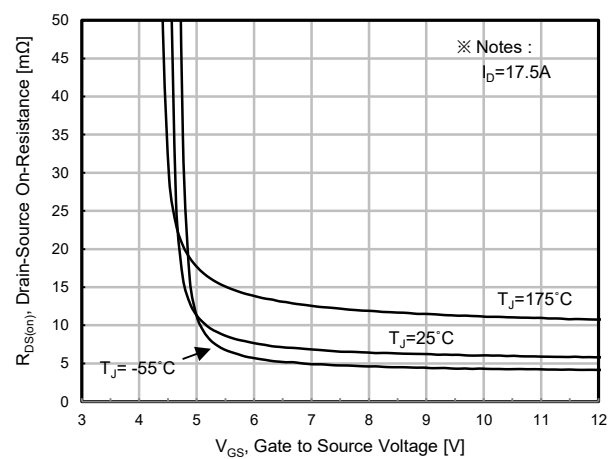


Fig. 4. On-Resistance vs. Gate to source Voltage

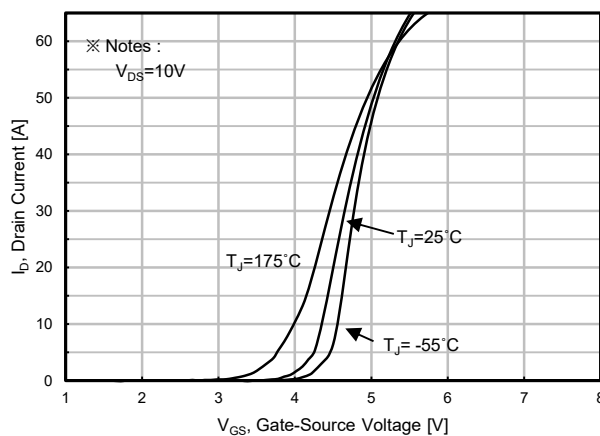


Fig. 5. Transfer Characteristics

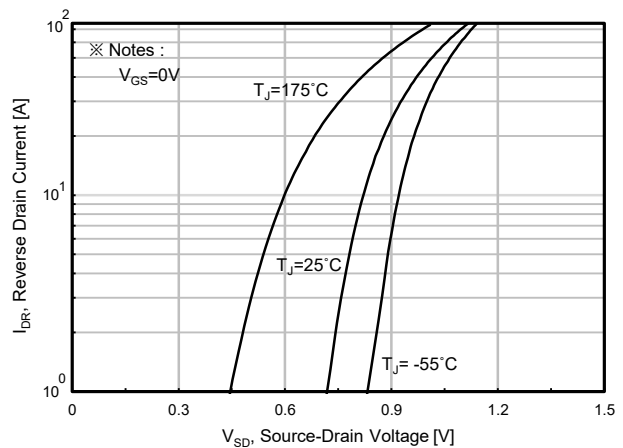


Fig. 6. Body Diode Forward Voltage Variation with Source Current and Temperature

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 °C, unless otherwise noted)

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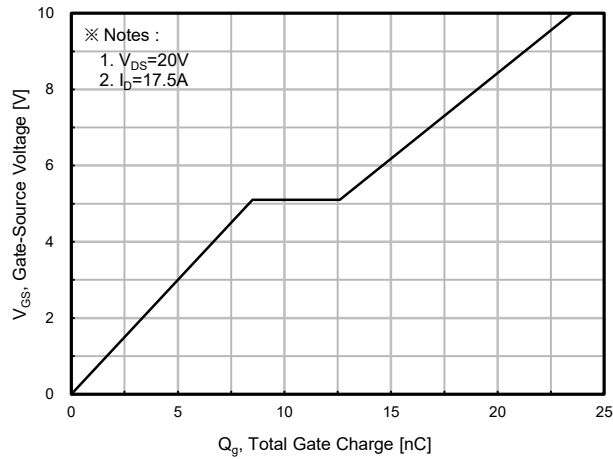


Fig. 7. Gate Charge

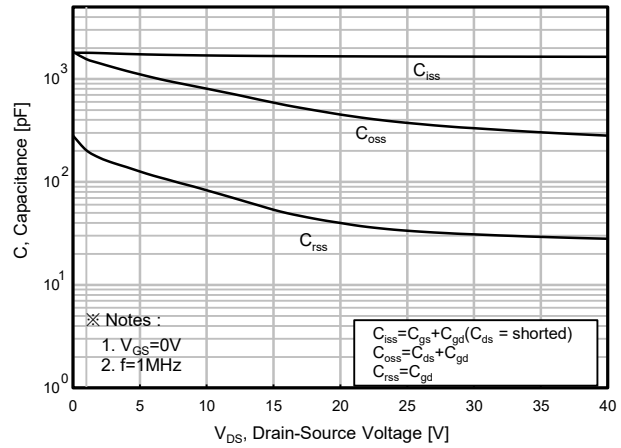


Fig. 8. Capacitance

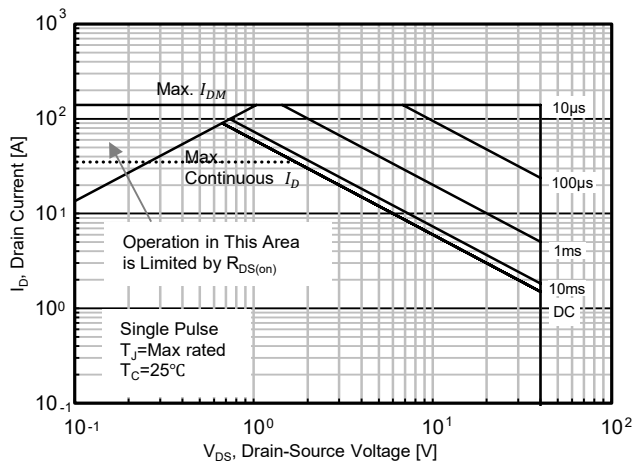


Fig. 9. Safe Operating Area, Junction-to-Ambient

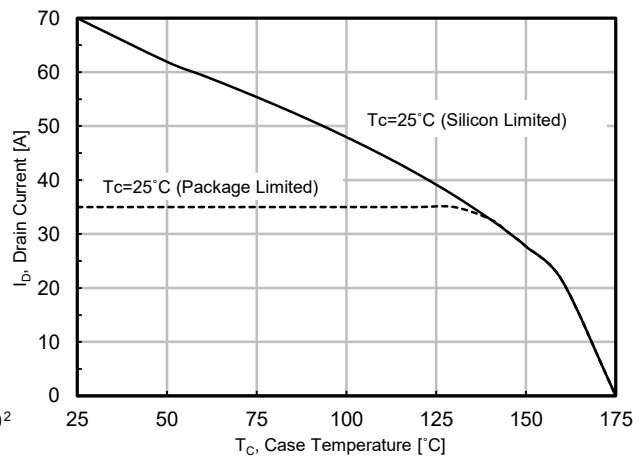
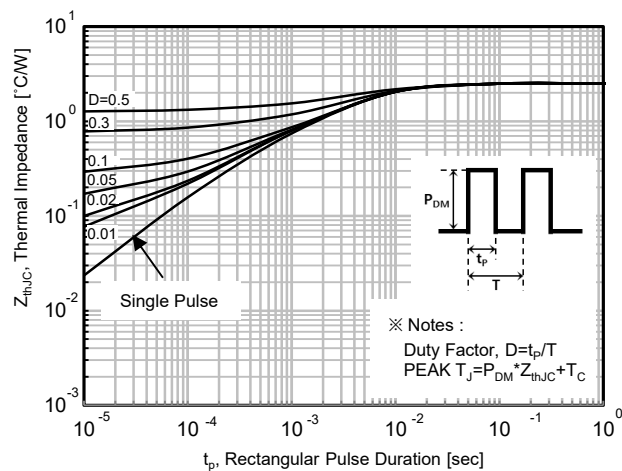
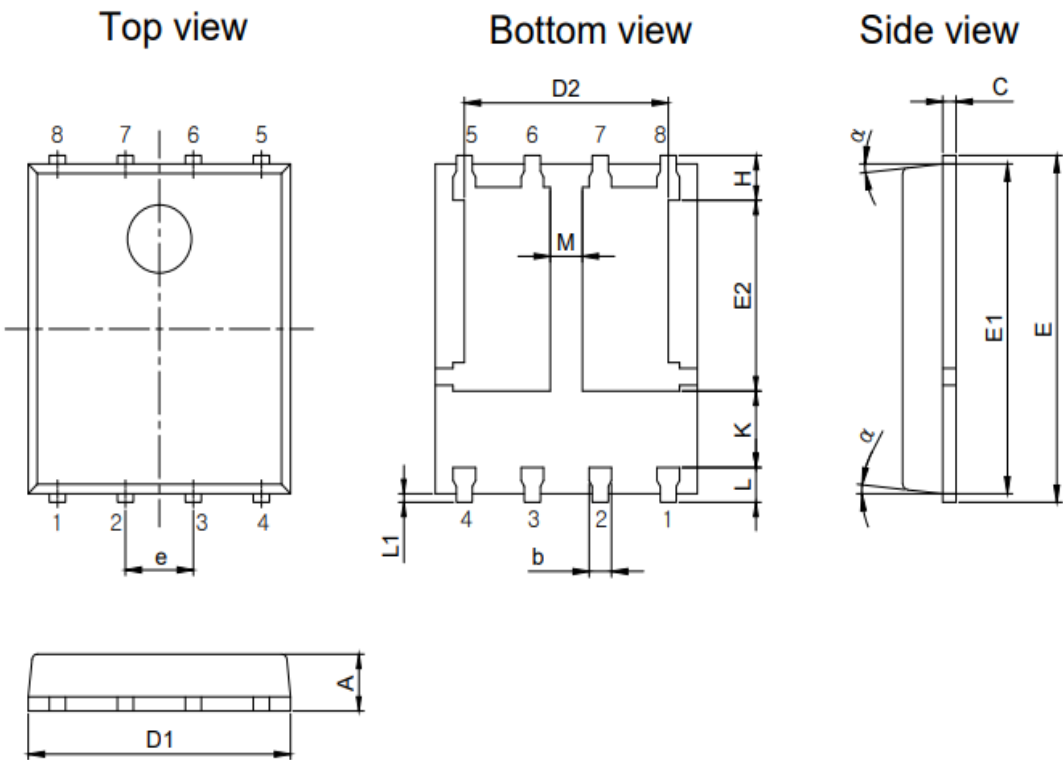


Fig. 10. Maximum Drain vs. Case Temperature

Fig. 11. Transient Thermal Impedance Junction to Case (R_{thjc})

Package information

PDFN56-DUAL



Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	–	–
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	–	–
α	0°	–	12°

Notes
Package body size, length and width do not include mold flash, protrusions and gate burrs.

DISCLAIMER :

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