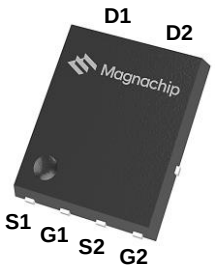
AMDUA040N070RH

Dual N-channel Trench MOSFET 40V 7.0mΩ 35A

FEATURES

- Trench power MOSFET technology
- N-channel, normal level
- 100% Avalanche tested
- Maximum 175°C junction temperature
- AEC-Q101 qualified



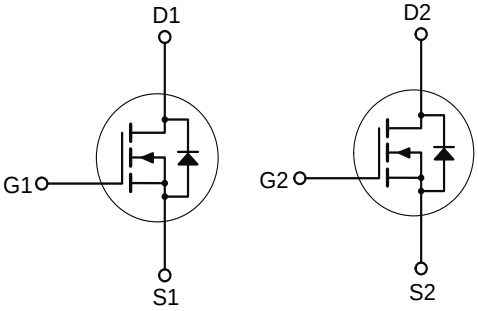
Top View

PDFN56-DUAL

Bottom View

APPLICATIONS

- Motor inverter
- Switching applications



KEY PERFORMANCE PARAMETERS

V_{DS}	40	V
$R_{DS(on),\ typ.}$	0.0061	Ω
I_D	35	A
Q_G	24	nC
Junction temperature, max	175	°C

RoHS Compliant
HALOGEN-FREE

ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
AMDUA040N070RH	PDFN56-DUAL	040N070	Tape & Reel	Halogen Free

http://www.magnachip.com/

ABSOLUTE MAXIMUM RATINGS, at T_C = 25°C, unless otherwise specified

PARAMETER		SYMBOL	RATING	UNIT
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain current	Tc=25°C (Silicon Limited)	I_D	70	A
	Tc=25°C (Package Limited)		35	A
	Tc=100°C (Silicon Limited)		49	A
	Tc=100°C (Package Limited)		35	A
[1] Pulsed drain current	Tc=25°C	I_{DM}	140	A
Total power dissipation	Tc=25°C	P_{tot}	60	W
	Tc=100°C		30	W
[2] Avalanche energy, single pulse		E_{AS}	45	mJ
Operating and storage temperature		T_j, T_{stg}	- 55 ~ 175	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATING	UNIT
Thermal resistance, junction - case	$R_{\theta JC}$	2.5	°C/W
[3] Thermal resistance, junction - ambient	$R_{\theta JA}$	100	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C)

STATIC CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=250 μA
Gate threshold voltage	$V_{GS(th)}$	2.45	3.20	3.95	V	V_{DS}=V_{GS}, I_D=250 μA
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=40 V, V_{GS}=0 V
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	V_{GS}=±20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	6.1	7.0	mΩ	V_{GS}=10 V, I_D=17.5 A
4) Gate resistance	R_G	-	2.3	-	Ω	f=1MHz
4) Transconductance	g_{fs}	-	42	-	S	V_{DS}=10 V, I_D=17.5 A

4) DYNAMIC CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Input capacitance	C_{iss}	-	1658	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance	C_{oss}	-	445	-	pF	
Reverse transfer capacitance	C_{rss}	-	41	-	pF	
Turn-on delay time	$t_{d(on)}$	-	17	-	ns	V_{DD}=20 V, V_{GS}=10 V, ID=17.5 A, $R_{G,ext}$=3Ω
Rise time	t_r	-	11	-	ns	
Turn-off delay time	$t_{d(off)}$	-	27	-	ns	
Fall time	t_f	-	9	-	ns	

4) GATE CHARGE CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Gate to source charge	Q_{gs}	-	9	-	nC	V_{DD}=20 V, I_D=17.5 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{gs(th)}$	-	5	-	nC	
Gate to drain charge	Q_{gd}	-	3	-	nC	
Switching charge	Q_{sw}	-	7	-	nC	
Gate charge total	Q_g	-	24	-	nC	
Gate plateau voltage	$V_{plateau}$	-	5.1	-	V	

SOURCE-DRAIN DIODE

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
4) Diode continous forward current	I_S	-	-	35	A	-
4) Diode pulse current	$I_{S,pulse}$	-	-	140	A	pulsed; tp ≤ 10 μs
Diode forward voltage	V_{SD}	-	0.9	1.2	V	V_{GS}=0 V, I_F=17.5 A
4) Reverse recovery time	t_{rr}	-	57.1	-	ns	I_F=17.5 A, d_{iF}/dt=100 A/μs
4) Reverse recovery charge	Q_{rr}	-	51.7	-	nC	

Notes

1. Pulse width limited by Tjmax
2. Starting TJ=25°C, L=1mH, I_{AS}=9.5A, V_{DD}=36V, V_{GS}=10V
3. Surface mounted FR-4 board by JEDEC (jesd51-7)
4. The parameter is not subject to production testing - guaranteed by design.

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 ℃, unless otherwise noted)

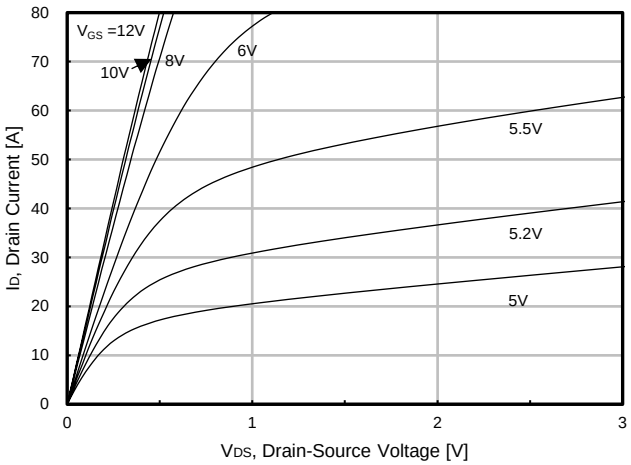


Fig. 1. Output Characteristics (25℃)

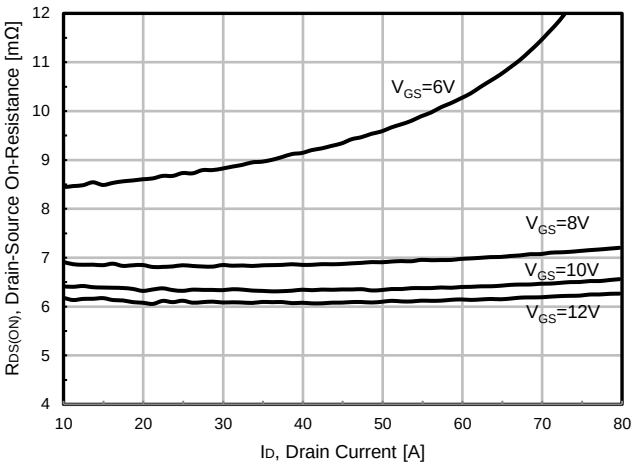


Fig. 2. Static On-Resistance Variation

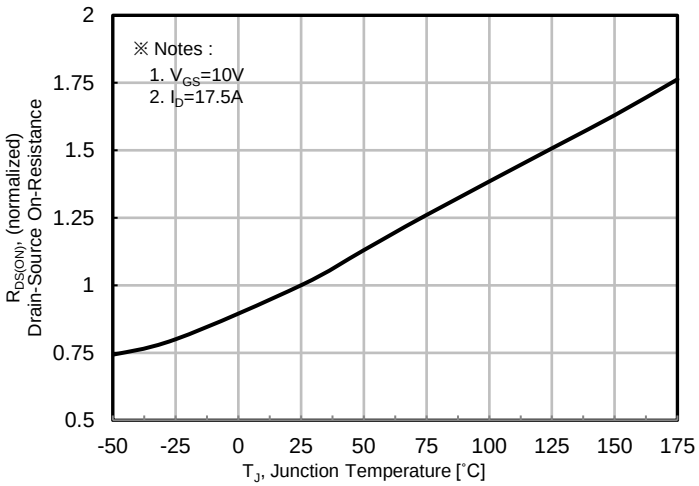


Fig. 3. On-Resistance vs. Junction Temperature

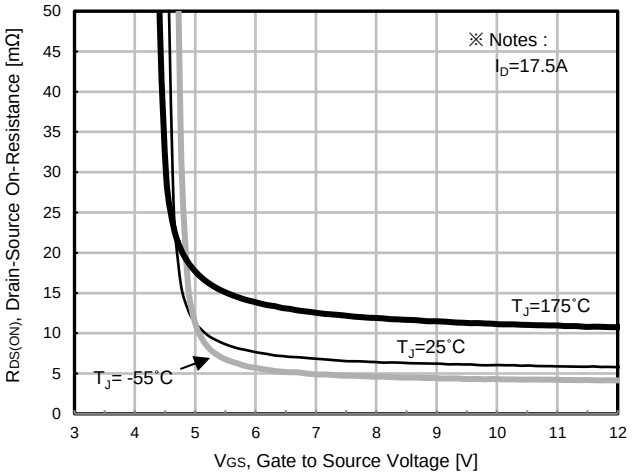


Fig. 4. On-Resistance vs. Gate to source Voltage

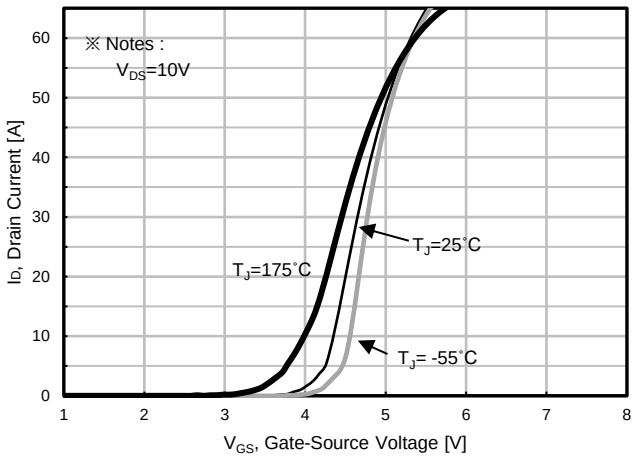


Fig. 5. Transfer Characteristics

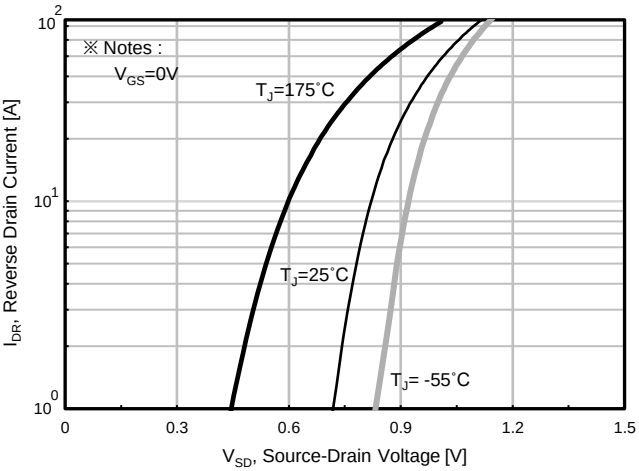


Fig. 6. Body Diode Forward Voltage Variation with Source Current and Temperature

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 ℃, unless otherwise noted)

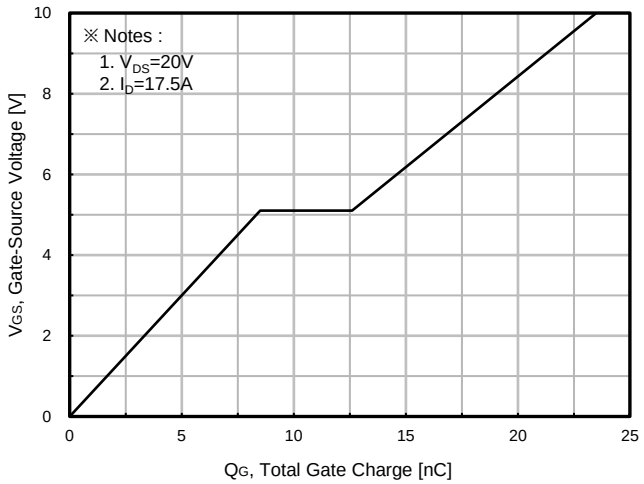


Fig. 7. Gate Charge

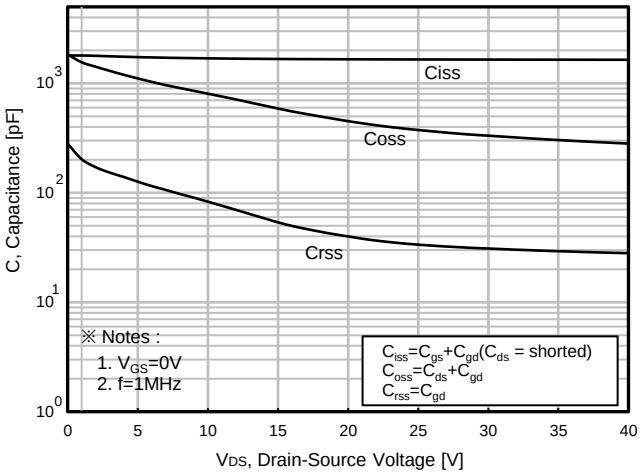


Fig. 8. Capacitance

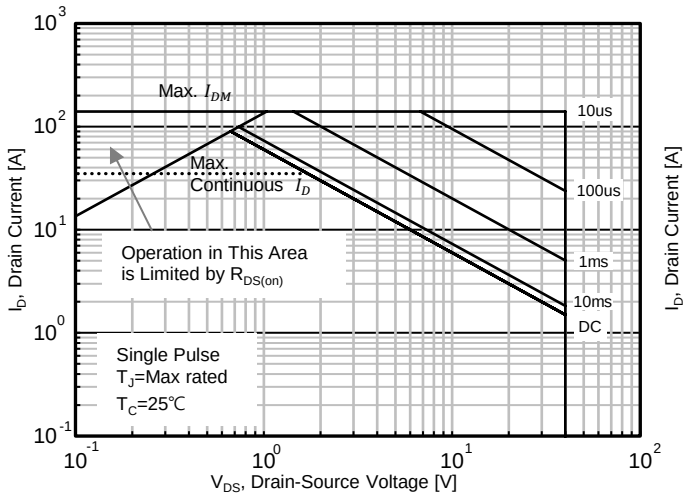


Fig. 9. Safe Operating Area, Junction-to-Ambient

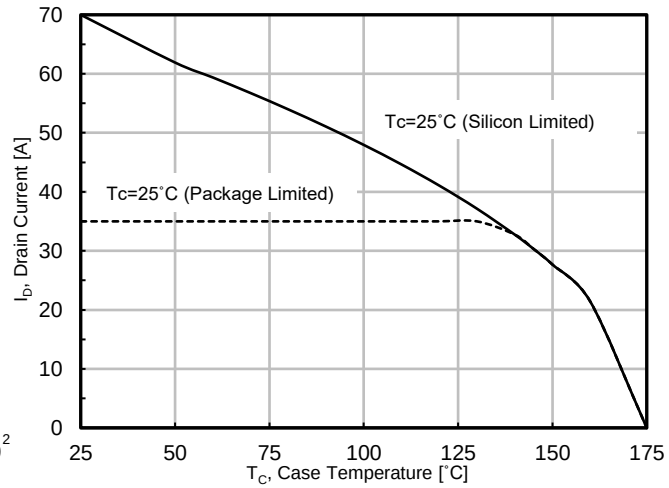


Fig. 10. Maximum Drain vs. Case Temperature

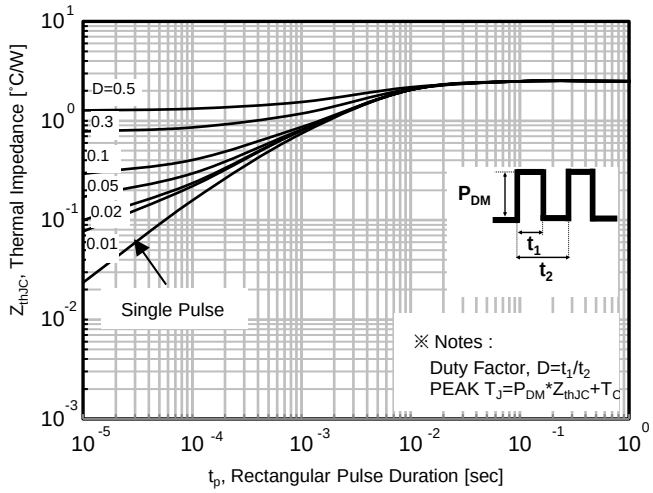
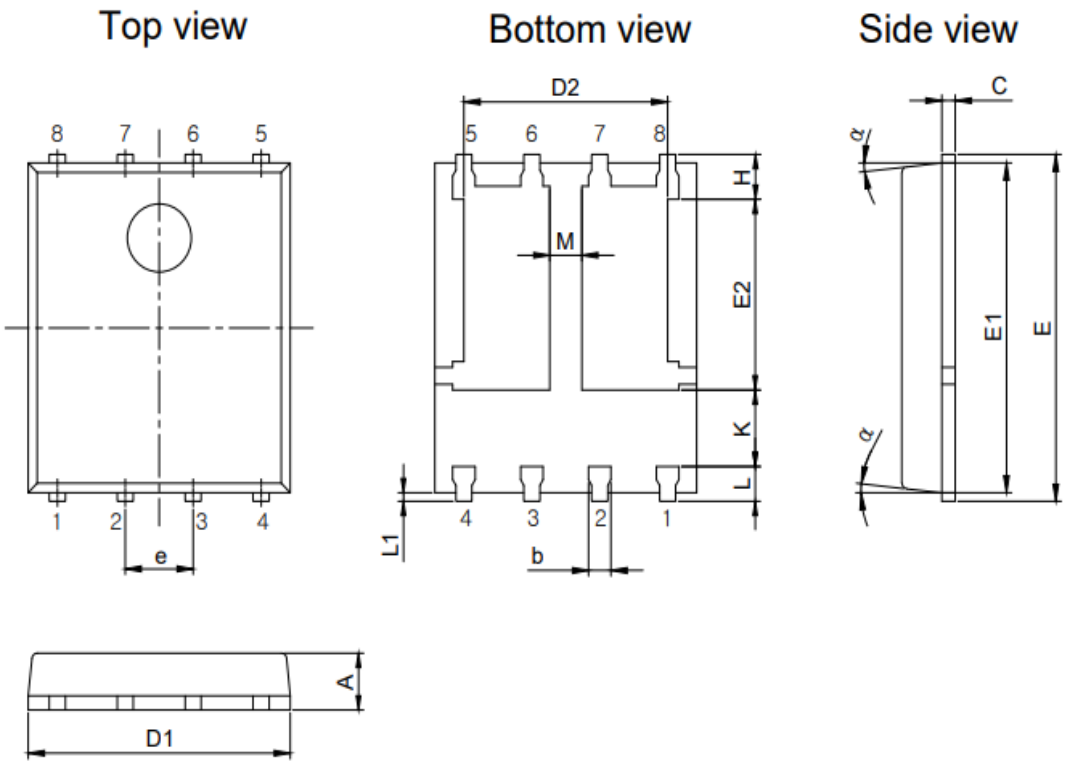


Fig. 11. Transient Thermal Impedance Junction to Case (Rthjc)

Package Outlines

PDFN56-DUAL



Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	–	–
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	–	–
α	0°	–	12°

Notes

Package body size, length and width do not include mold flash, protrusions and gate burrs.

DISCLAIMER :

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.