

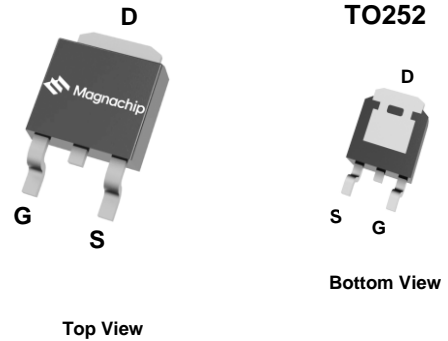


AMDD040P069RH

Single P-channel Trench MOSFET -40V 6.9mΩ -90A

FEATURES

- Trench power MOSFET technology
- P-channel, logic level
- 100% Avalanche tested
- Maximum 175°C junction temperature
- AEC-Q101 qualified

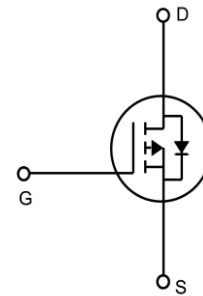


APPLICATIONS

- DC/DC and AC/DC converters
- Switching applications

KEY PERFORMANCE PARAMETERS

V_{DS}	-40	V
$R_{DS(on), typ.}$	0.0062	Ω
I_D (Package limited)	-90	A
Q_G	91	nC
Junction temperature, max.	175	$^{\circ}C$



ORDERING INFORMATION

Type / Ordering Code	Package	Marking	Packing	RoHS Status
AMDD040P069RH	TO252	040P069	Tape & Reel	Halogen Free

<http://www.magnachip.com/>

ABSOLUTE MAXIMUM RATINGS, at $T_C = 25^\circ\text{C}$, unless otherwise specified

PARAMETER		SYMBOL	RATING	UNIT
Drain-source Voltage		V_{DS}	-40	V
Gate-source Voltage		V_{GS}	± 18	V
Drain current	$T_C=25^\circ\text{C}$ (Package limited)	I_D	-90	A
	$T_C=25^\circ\text{C}$ (Silicon limited)		-104	A
	$T_C=100^\circ\text{C}$		-73	A
¹⁾ Pulsed drain current	$T_C=25^\circ\text{C}$	I_{DM}	-360	A
Total power dissipation	$T_C=25^\circ\text{C}$	P_{tot}	115	W
	$T_C=100^\circ\text{C}$		58	W
²⁾ Avalanche energy, single pulse		E_{AS}	153	mJ
Operating and storage temperature		T_j, T_{stg}	- 55 ~ 175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	RATING	UNIT
Thermal resistance, junction - case		$R_{\theta JC}$	1.3	$^\circ\text{C/W}$
³⁾ Thermal resistance, junction - ambient		$R_{\theta JA}$	50	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS (T_J = 25°C)

STATIC CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Drain-source breakdown voltage	V _{(BR)DSS}	-40	-	-	V	V _{GS} =0 V, I _D =-250 μA
Gate threshold voltage	V _{GS(th)}	-1.1	-1.8	-2.8		V _{DS} =V _{GS} , I _D =-250 μA
Zero gate voltage drain current	I _{DSS}	-	-	1	μA	V _{DS} =-40 V, V _{GS} =0 V
Gate-source leakage current	I _{GSS}	-	-	± 100	nA	V _{GS} =±18 V, V _{DS} =0 V
Drain-source on-state resistance	R _{DS(on)}	-	6.2	6.9	mΩ	V _{GS} =-10 V, I _D =-45 A
		-	8.4	15.4		V _{GS} =-4.5 V, I _D =-27 A
⁴⁾ Gate resistance	R _G	-	8.5	-	Ω	f=1MHz
⁴⁾ Transconductance	g _{fs}	-	80	-	S	V _{DS} =-10 V, I _D =-45 A

⁴⁾ DYNAMIC CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Input capacitance	C _{iss}	-	4,374	-	pF	V _{GS} =0 V, V _{DS} =-20 V, f=1 MHz
Output capacitance	C _{oss}	-	701	-		
Reverse transfer capacitance	C _{rss}	-	373	-		
Turn-on delay time	t _{d(on)}	-	17	-	ns	V _{DD} =-20 V, V _{GS} =-10 V, I _D =-45 A, R _{G,ext} =3Ω
Rise time	t _r	-	9	-		
Turn-off delay time	t _{d(off)}	-	112	-		
Fall time	t _f	-	57	-		

⁴⁾ GATE CHARGE CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Gate to source charge	Q _{gs}	-	17	-	nC	V _{DD} =-20 V, I _D =-45 A, V _{GS} =0 to -10 V
Gate charge at threshold	Q _{gs(th)}	-	7	-		
Gate to drain charge	Q _{gd}	-	17	-		
Switching charge	Q _{sw}	-	26	-		
Gate charge total	Q _g	-	41	-		
		-	91	-		
Gate plateau voltage	V _{plateau}	-	-3.7	-	V	

SOURCE-DRAIN DIODE

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
⁴⁾ Diode continuous forward current	I _S	-	-	-90	A	-
⁴⁾ Diode pulse current	I _{S,pulse}	-	-	-360		pulsed; t _p ≤ 10 μs
Diode forward voltage	V _{SD}	-	-0.9	-1.2	V	V _{GS} =0 V, I _F =-45 A
⁴⁾ Reverse recovery time	t _{rr}	-	81	-	ns	I _F =-45 A, dI _F /dt=100 A/μs
⁴⁾ Reverse recovery charge	Q _{rr}	-	101	-	nC	

Notes

- Pulse width limited by T_{Jmax}
- Starting T_J=25°C, L=1mH, I_{AS}=-16.5A, V_{DD}=-20V, V_{GS}=-10V
- Surface mounted FR-4 board by JEDEC (jesd51-7)
- The parameter is not subject to production testing - guaranteed by design.

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 °C, unless otherwise noted)

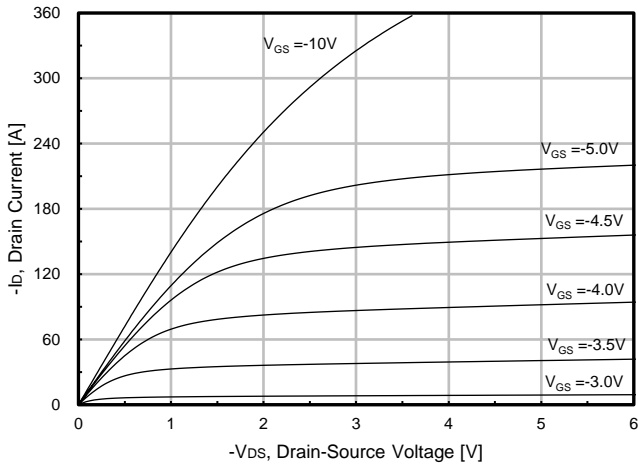


Fig. 1. Output Characteristics (25°C)

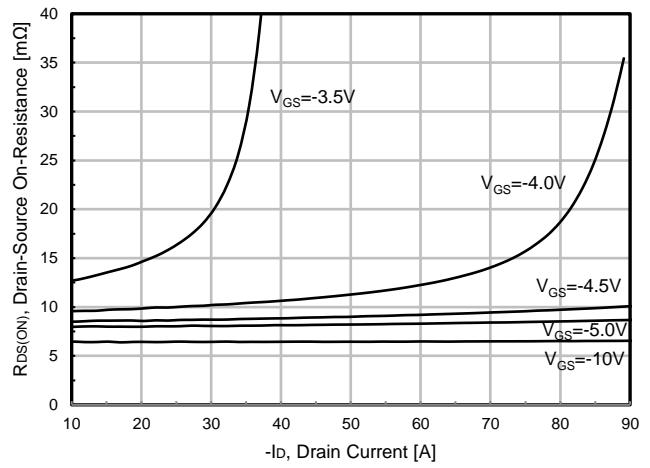


Fig. 2. Static On-Resistance Variation

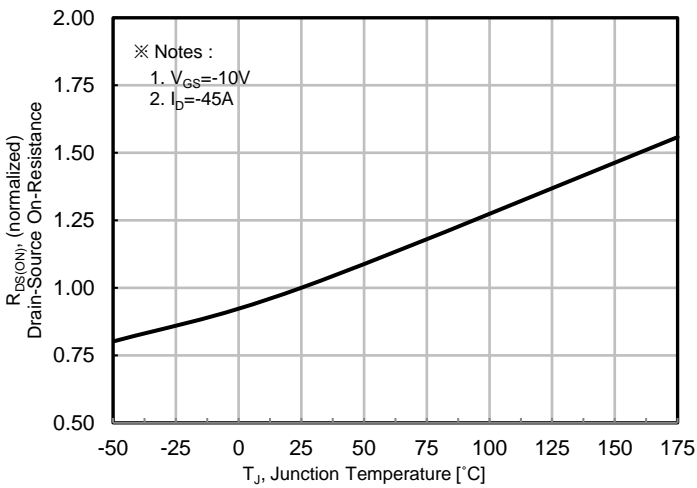


Fig. 3. On-Resistance vs. Junction Temperature

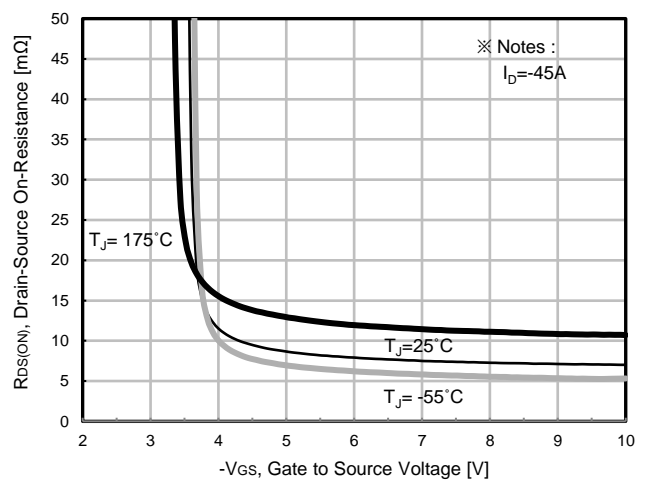


Fig. 4. On-Resistance vs. Gate to source Voltage

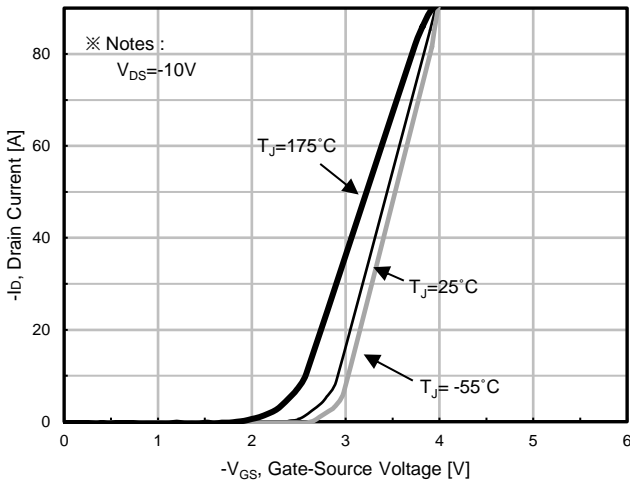


Fig. 5. Transfer Characteristics

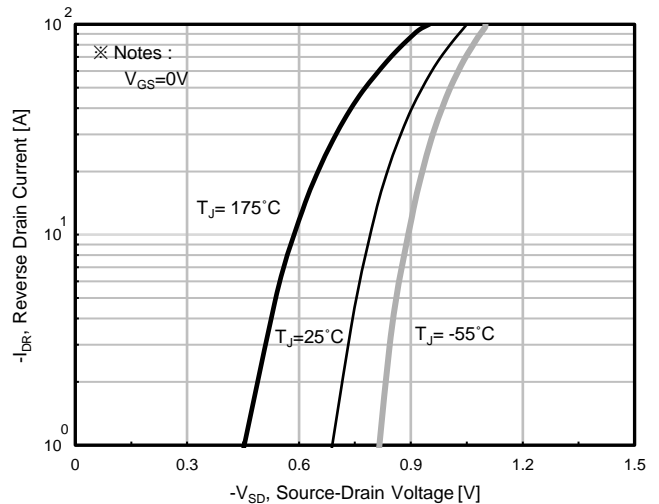


Fig. 6. Body Diode Forward Voltage Variation with Source Current and Temperature

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 °C, unless otherwise noted)

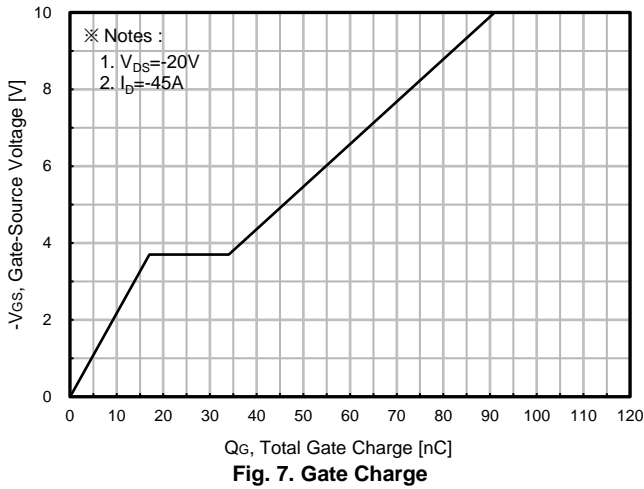


Fig. 7. Gate Charge

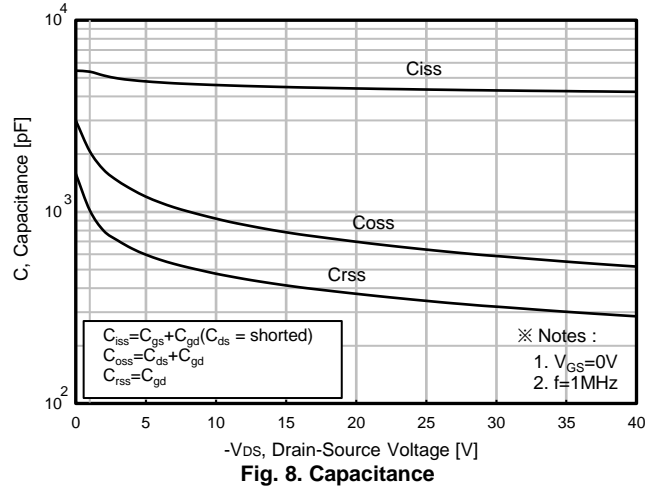


Fig. 8. Capacitance

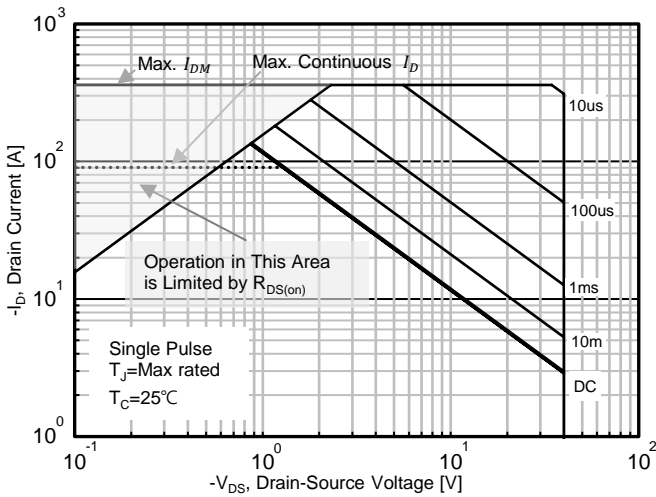


Fig. 9. Safe Operating Area, Junction-to-Ambient

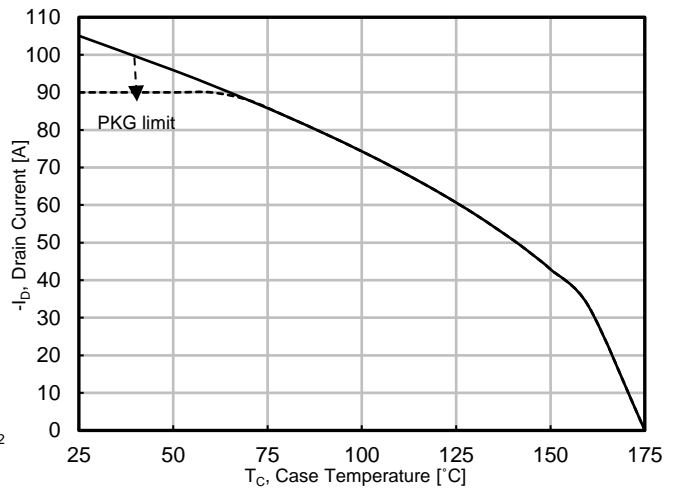


Fig. 10. Maximum Drain vs. Case Temperature

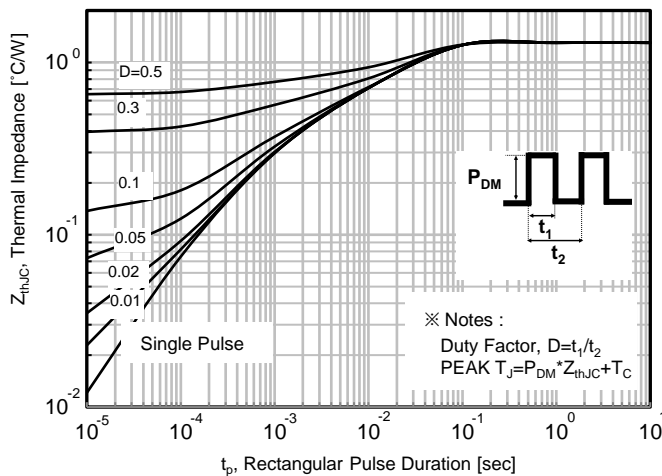
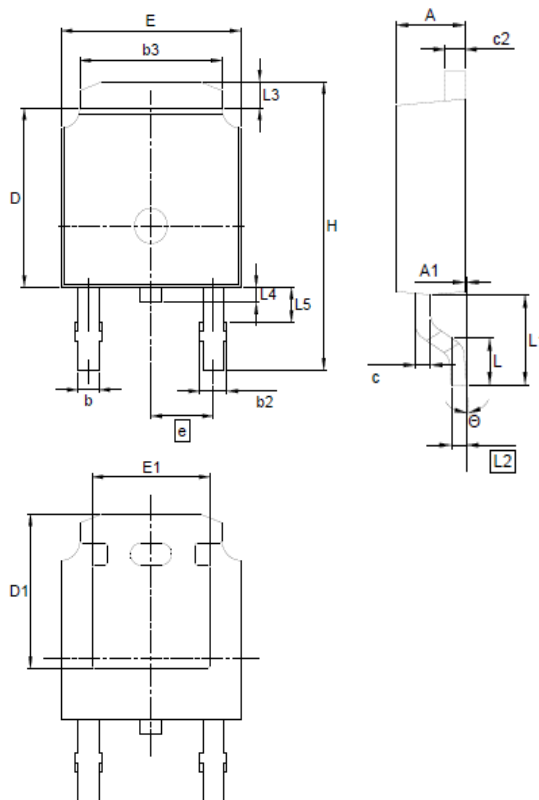


Fig. 11. Transient Thermal Impedance Junction to Case (Rthjc)

Package information

T0252




Dim (mm)	MX			ATX		
	Min	Nom	Max	Min	Nom	Max
E	6.35	-	6.73	6.35	-	6.73
L	1.40	1.52	1.78	1.50	-	1.78
L1	2.74REF			2.74REF		
L2	0.508BSC			0.508BSC		
L3	0.89	-	1.27	0.89	-	1.27
L4	-	-	1.02	-	-	1.02
L5	1.14	-	1.52	1.14	-	1.492
D	5.97	6.10	6.22	5.97	-	6.22
H	9.40	-	10.41	9.94	-	10.34
b	0.64	-	0.89	0.65	-	0.884
b2	0.76	-	1.14	0.76	-	1.124
b3	4.95	-	5.46	4.95	-	5.46
e	2.286BSC			2.286BSC		
A	2.18	-	2.39	2.18	-	2.39
A1	-	-	0.13	-	-	0.13
c	0.46	-	0.61	0.46	-	0.61
c2	0.46	-	0.89	0.46	-	0.60
D1	5.21	-	-	5.21	-	-
E1	4.32	-	-	4.32	-	-
Ø	0.00	-	10.00	0.00	-	10.00

Notes

Package body size, length and width do not include mold flash, protrusions and gate burrs.

DISCLAIMER :

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

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