

MMP65R190P

650V 0.19 Ω N-channel MOSFET

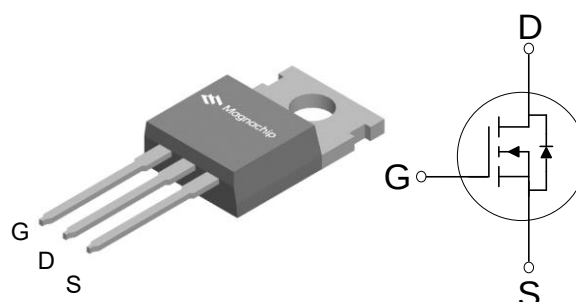
Description

MMP65R190P is power MOSFET using Magnachip's advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI to designers as well as low switching loss.

Key Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	0.19	Ω
$V_{TH,typ}$	3	V
I_D	20	A
$Q_{g,typ}$	53	nC

Package & Internal Circuit



Features

- Low Power Loss by High Speed Switching and Low On-Resistance
- 100% Avalanche Tested
- Green Package – Pb Free Plating, Halogen Free

Applications

- PFC Power Supply Stages
- Switching Applications
- Adapter
- Motor Control
- DC – DC Converters

Ordering Information

Order Code	Marking	Temp. Range	Package	Packing	RoHS Status
MMP65R190PTH	65R190P	-55 ~ 150 $^{\circ}$ C	TO-220	Tube	Halogen Free

■ Absolute Maximum Rating ($T_c=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit	Note
Drain – Source voltage	V_{DSS}	650	V	
Gate – Source voltage	V_{GSS}	± 30	V	
Continuous drain current	I_{D}	20	A	$T_c=25^{\circ}\text{C}$
		12.7	A	$T_c=100^{\circ}\text{C}$
Pulsed drain current ⁽¹⁾	I_{DM}	60	A	
Power dissipation	P_{D}	154	W	
Single - pulse avalanche energy	E_{AS}	485	mJ	
MOSFET dv/dt ruggedness	dv/dt	50	V/ns	
Diode dv/dt ruggedness	dv/dt	15	V/ns	
Storage temperature	T_{stg}	-55 ~150	$^{\circ}\text{C}$	
Maximum operating junction temperature	T_{j}	150	$^{\circ}\text{C}$	

1) Pulse width t_p limited by $T_{\text{j,max}}$

2) $I_{\text{SD}} \leq I_{\text{D}}, V_{\text{DS peak}} \leq V_{(\text{BR})\text{DSS}}$

■ Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case max	R_{thjc}	0.81	$^{\circ}\text{C/W}$
Thermal resistance, junction-ambient max	R_{thja}	62.5	$^{\circ}\text{C/W}$

■ Static Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain – Source Breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS} = 0V, I_D=0.25mA$
Gate Threshold Voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS} = V_{GS}, I_D=0.25mA$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS} = 700V, V_{GS} = 0V$
Gate Leakage Current	I_{GSS}	-	-	100	nA	$V_{GS} = \pm 30V, V_{DS} = 0V$
Drain-Source On State Resistance	$R_{DS(ON)}$	-	0.17	0.19	Ω	$V_{GS} = 10V, I_D = 10 A$

■ Dynamic Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{iss}	-	1860	-	pF	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz$
Output Capacitance	C_{oss}	-	1425	-		
Reverse Transfer Capacitance	C_{rss}	-	76	-		
Effective Output Capacitance Energy Related ⁽³⁾	$C_{o(er)}$	-	39	-		$V_{DS} = 0V \text{ to } 560V, V_{GS} = 0V, f = 1.0MHz$
Turn On Delay Time	$t_{d(on)}$	-	40	-	ns	$V_{GS} = 10V, R_G = 25\Omega, V_{DS} = 350V, I_D = 20 A$
Rise Time	t_r	-	75	-		
Turn Off Delay Time	$t_{d(off)}$	-	172	-		
Fall Time	t_f	-	54	-		
Total Gate Charge	Q_g	-	53	-	nC	$V_{GS} = 10V, V_{DS} = 560V, I_D = 20 A$
Gate – Source Charge	Q_{gs}	-	13	-		
Gate – Drain Charge	Q_{gd}	-	20	-		
Gate Resistance	R_G	-	3.0	-	Ω	$V_{GS} = 0V, f = 1.0MHz$

3) $C_{o(er)}$ is a capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0V to 80% $V_{(BR)DSS}$

■ Reverse Diode Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Continuous Diode Forward Current	I_{SD}	-	-	20	A	
Diode Forward Voltage	V_{SD}	-	-	1.4	V	$I_{SD} = 20\text{ A}$, $V_{GS} = 0\text{ V}$
Reverse Recovery Time	t_{rr}	-	524	-	ns	$I_{SD} = 20\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$
Reverse Recovery Charge	Q_{rr}	-	9.4	-	μC	
Reverse Recovery Current	I_{rrm}	-	35.7	-	A	

■ Characteristic Graph

Fig.1 On-Region Characteristics.

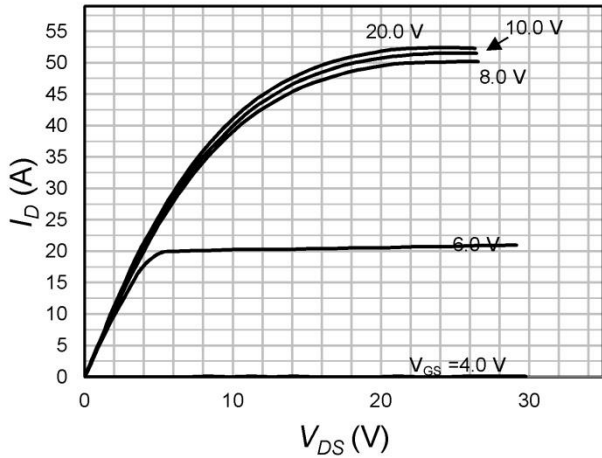


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

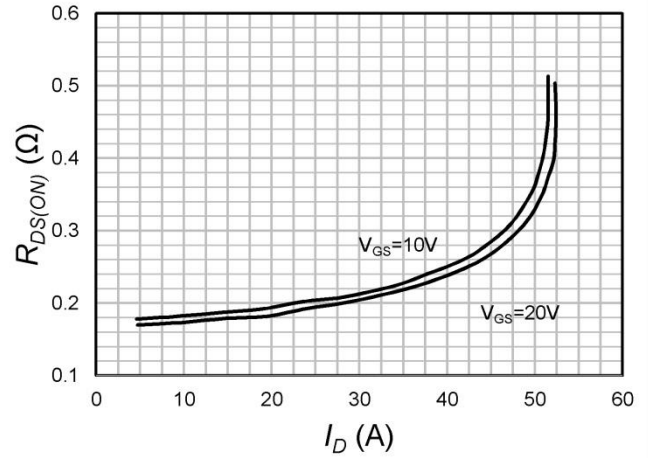


Fig.3 On-Resistance Variation with Temperature (Normalized)

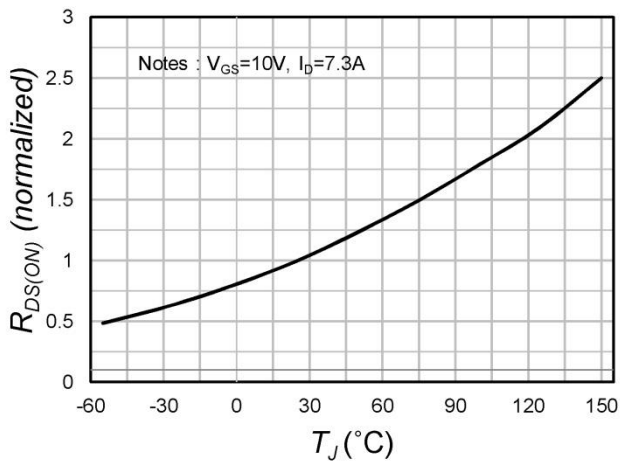


Fig.4 Breakdown Voltage Variation vs. Temperature (Normalized)

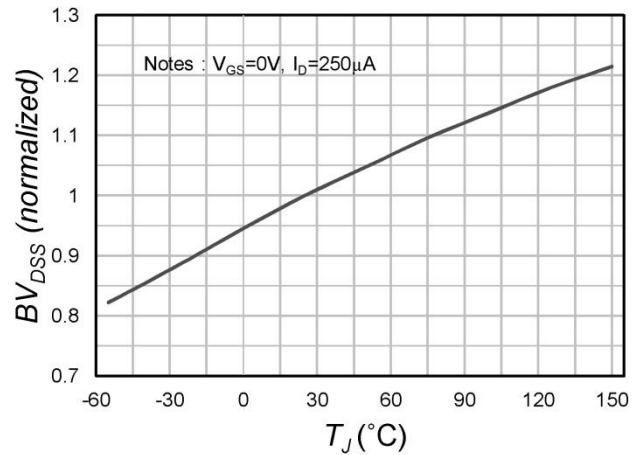


Fig.5 Transfer Characteristics

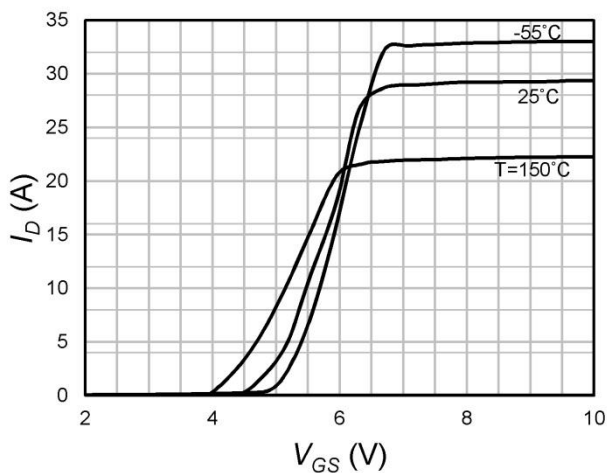


Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature

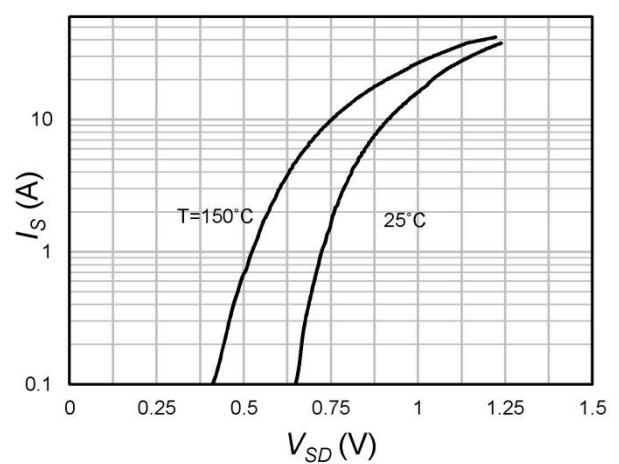


Fig.7 Gate Charge Characteristics

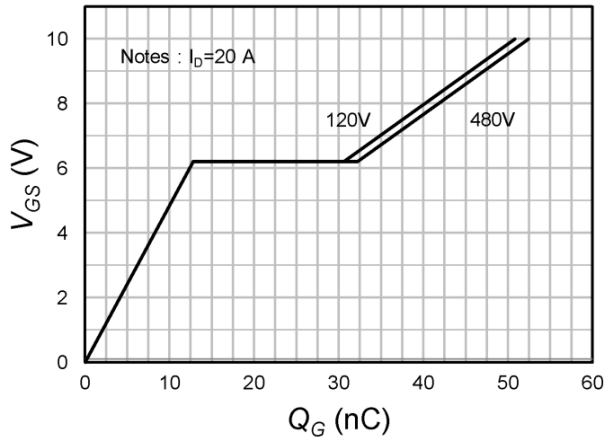


Fig.8 Capacitance Characteristics

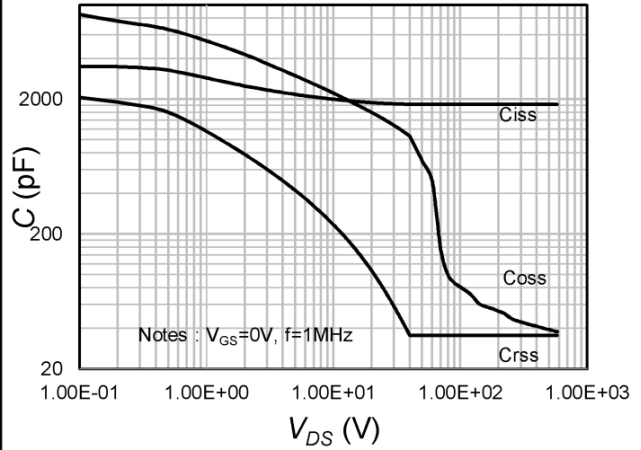
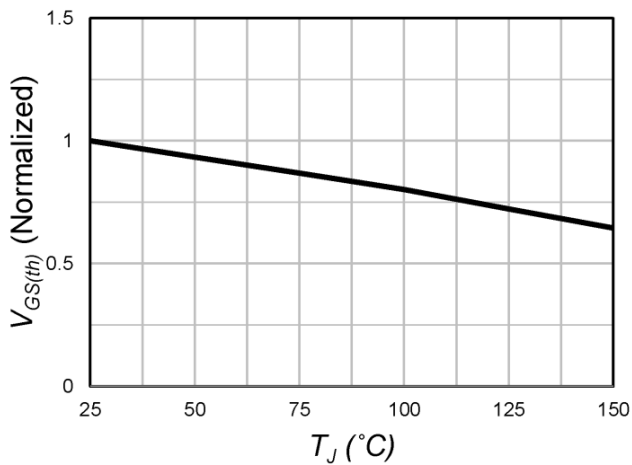

Fig.9 $V_{GS(th)}$ Variation with Temperature (Normalized)


Fig.10 Maximum Drain Current vs. Case Temperature

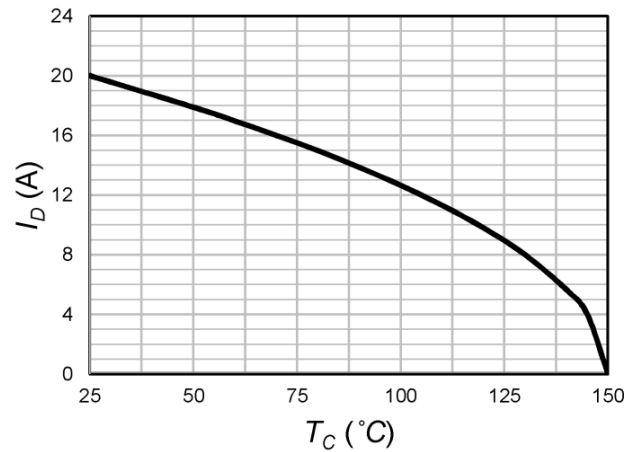


Fig.11 Single Pulse Maximum Power Dissipation

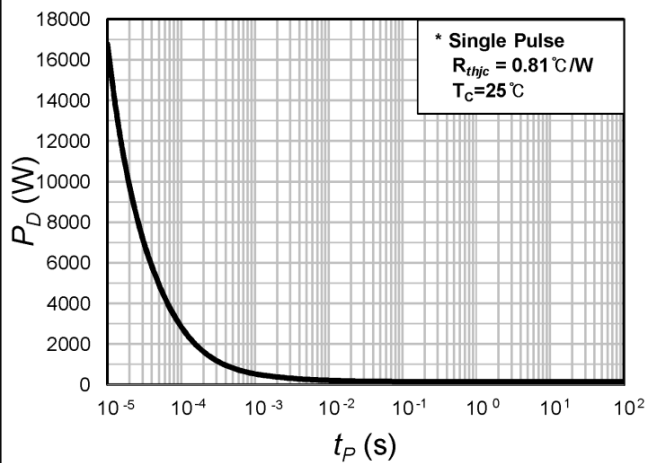


Fig.12 Output Capacitance Stored Energy

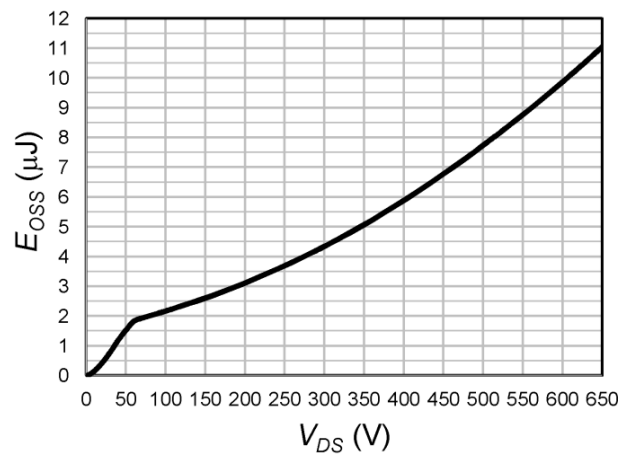


Fig.13 Transient Thermal Response Curve

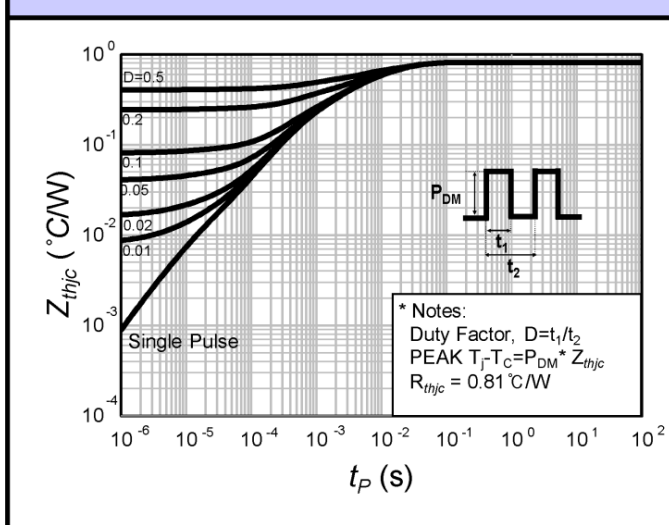
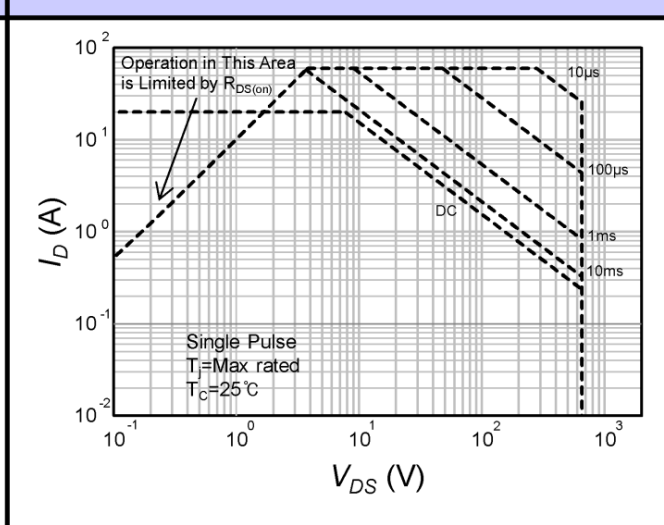


Fig.14 Maximum Safe Operating Area



■ Test Circuit

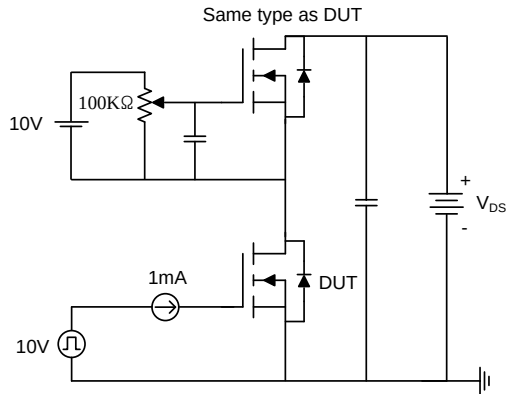


Fig15-1. Gate charge measurement circuit

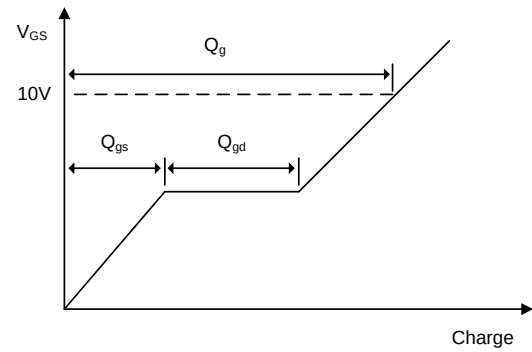


Fig15-2. Gate charge waveform

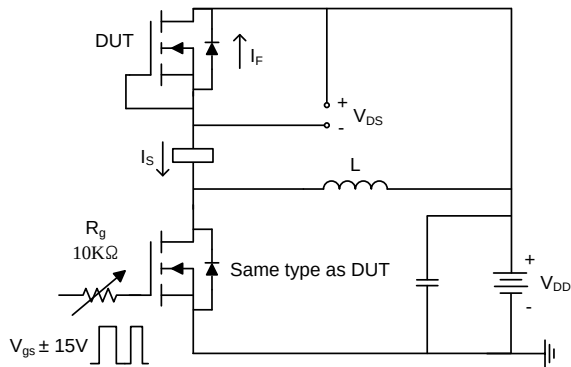


Fig16-1. Diode reverse recovery test circuit

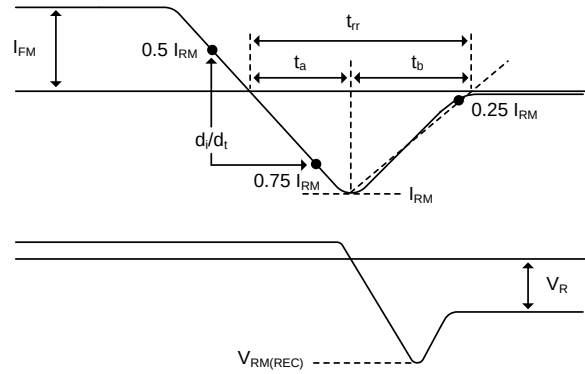


Fig16-1. Diode reverse recovery test waveform

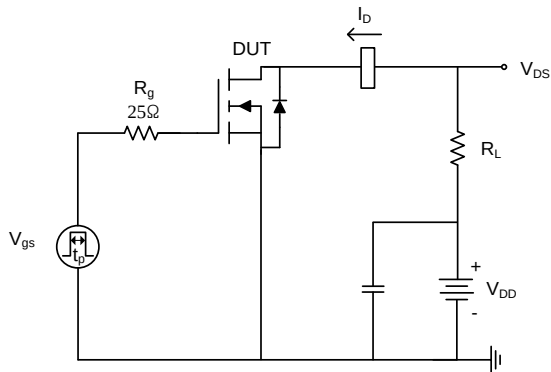


Fig17-1. Switching time test circuit for resistive load

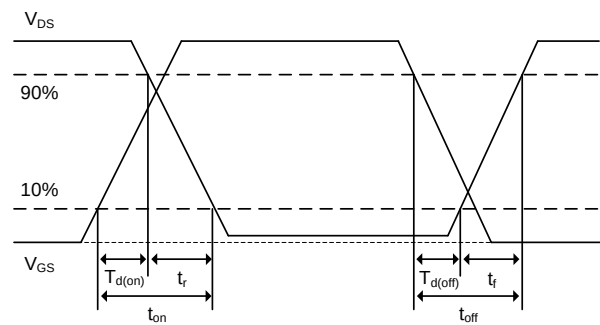


Fig17-2. Switching time waveform

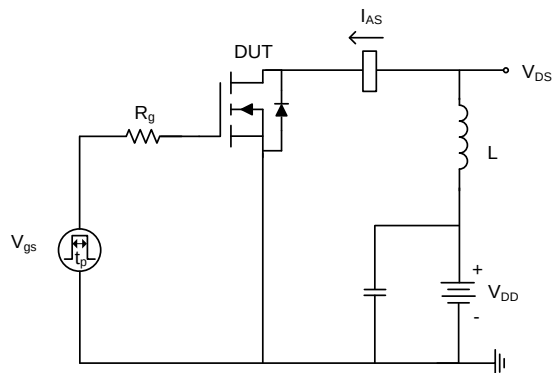


Fig18-1. Unclamped inductive load test circuit

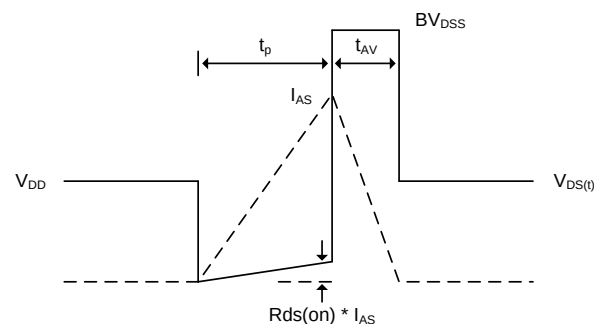
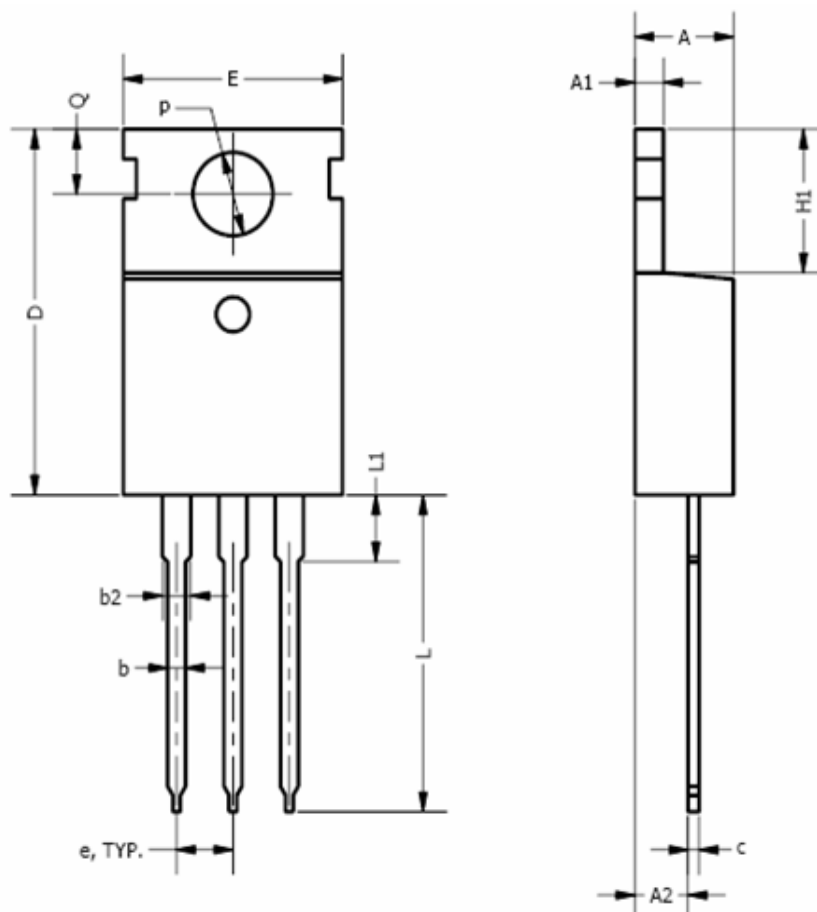


Fig18-2. Unclamped inductive waveform

■ Physical Dimension

3 Leads, TO-220

Dimensions are in millimeters unless otherwise specified



Symbol	Min	Nom	Max
A	3.56		4.83
A1	0.50		1.40
A2	2.03		2.92
b	0.38	0.69	1.02
b2	1.14	1.45	1.78
c	0.36		0.61
D	14.22		16.51
e	2.54 TYP		
E	9.65		10.67
H1	5.84		6.86
L	12.70		14.73
L1			6.35
Φ P	3.53		4.09
Q	2.54		3.43

Note : Package body size, length and width do not include mold flash, protrusions and gate burrs.

DISCLAIMER:

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

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