

# MMIS70R900P

## 700V 0.9Ω N-channel MOSFET

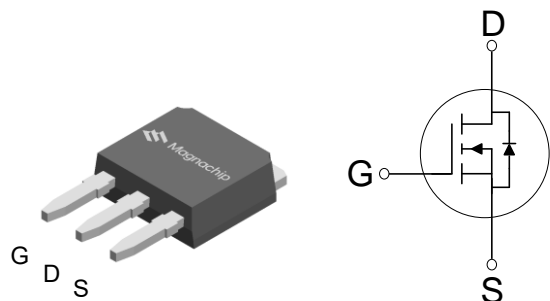
### ■ Description

MMIS70R900P is power MOSFET using Magnachip's advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI to designers as well as low switching loss.

### ■ Key Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	750	V
$R_{DS(on),max}$	0.9	Ω
$V_{TH,typ}$	3	V
$I_D$	5	A
$Q_{g,typ}$	15	nC

### ■ Package & Internal Circuit



### ■ Features

- Low Power Loss by High Speed Switching and Low On-Resistance
- 100% Avalanche Tested
- Green Package – Pb Free Plating, Halogen Free

### ■ Applications

- PFC Power Supply Stages
- Switching Applications
- Adapter
- Motor Control
- DC – DC Converters

### ■ Ordering Information

Order Code	Marking	Temp. Range	Package	Packing	RoHS Status
MMIS70R900PTH	70R900P	-55 ~ 150 °C	TO-251-VS (IPAK-VS)	Tube	Halogen Free

**■ Absolute Maximum Rating ( $T_c=25^\circ\text{C}$  unless otherwise specified)**

Parameter	Symbol	Rating	Unit	Note
Drain – Source voltage	$V_{DSS}$	700	V	
Gate – Source voltage	$V_{GSS}$	$\pm 30$	V	
Continuous drain current	$I_D$	5	A	$T_c=25^\circ\text{C}$
		3	A	$T_c=100^\circ\text{C}$
Pulsed drain current <sup>(1)</sup>	$I_{DM}$	15	A	
Power dissipation	$P_D$	40	W	
Single - pulse avalanche energy	$E_{AS}$	50	mJ	
MOSFET dv/dt ruggedness	dv/dt	50	V/ns	
Diode dv/dt ruggedness	dv/dt	15	V/ns	
Storage temperature	$T_{stg}$	-55 ~150	$^\circ\text{C}$	
Maximum operating junction temperature	$T_j$	150	$^\circ\text{C}$	

1) Pulse width  $t_P$  limited by  $T_{j,max}$

2)  $I_{SD} \leq I_D$ ,  $V_{DS\ peak} \leq V_{(BR)DSS}$

**■ Thermal Characteristics**

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case max	$R_{thjc}$	3.1	$^\circ\text{C}/\text{W}$
Thermal resistance, junction-ambient max	$R_{thja}$	62.5	$^\circ\text{C}/\text{W}$

**■ Static Characteristics ( $T_c=25^\circ\text{C}$  unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain – Source Breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	$V_{GS} = 0V$ , $I_D=0.25\text{mA}$
Gate Threshold Voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS} = V_{GS}$ , $I_D=0.25\text{mA}$
Zero Gate Voltage Drain Current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS} = 700V$ , $V_{GS} = 0V$
Gate Leakage Current	$I_{GSS}$	-	-	100	nA	$V_{GS} = \pm 30V$ , $V_{DS} = 0V$

Drain-Source On State Resistance	$R_{DS(ON)}$	-	0.81	0.9	$\Omega$	$V_{GS} = 10V, I_D = 1.5A$
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**■ Dynamic Characteristics ( $T_c=25^\circ C$  unless otherwise specified)**

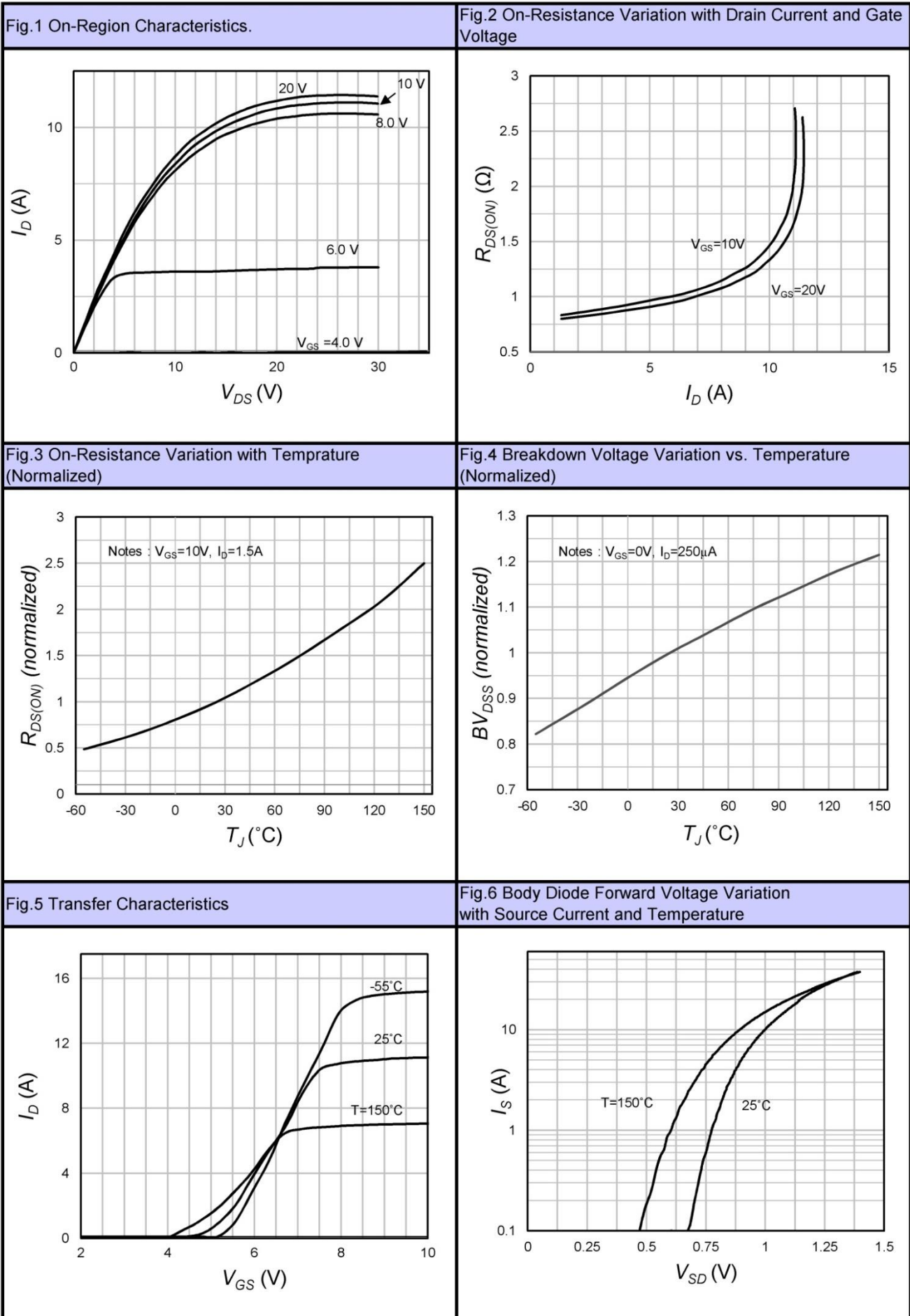
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	$C_{iss}$	-	430	-	pF	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz$
Output Capacitance	$C_{oss}$	-	330	-		
Reverse Transfer Capacitance	$C_{rss}$	-	19	-		
Effective Output Capacitance Energy Related <sup>(3)</sup>	$C_{o(er)}$	-	15	-		
Turn On Delay Time	$t_{d(on)}$	-	11	-	ns	$V_{GS} = 10V, R_G = 25\Omega, V_{DS} = 350V, I_D = 5A$
Rise Time	$t_r$	-	25	-		
Turn Off Delay Time	$t_{d(off)}$	-	37	-		
Fall Time	$t_f$	-	21	-		
Total Gate Charge	$Q_g$	-	15	-	nC	$V_{GS} = 10V, V_{DS} = 560V, I_D = 5A$
Gate – Source Charge	$Q_{gs}$	-	3	-		
Gate – Drain Charge	$Q_{gd}$	-	6	-		
Gate Resistance	$R_G$	-	5	-	$\Omega$	$V_{GS} = 0V, f = 1.0MHz$

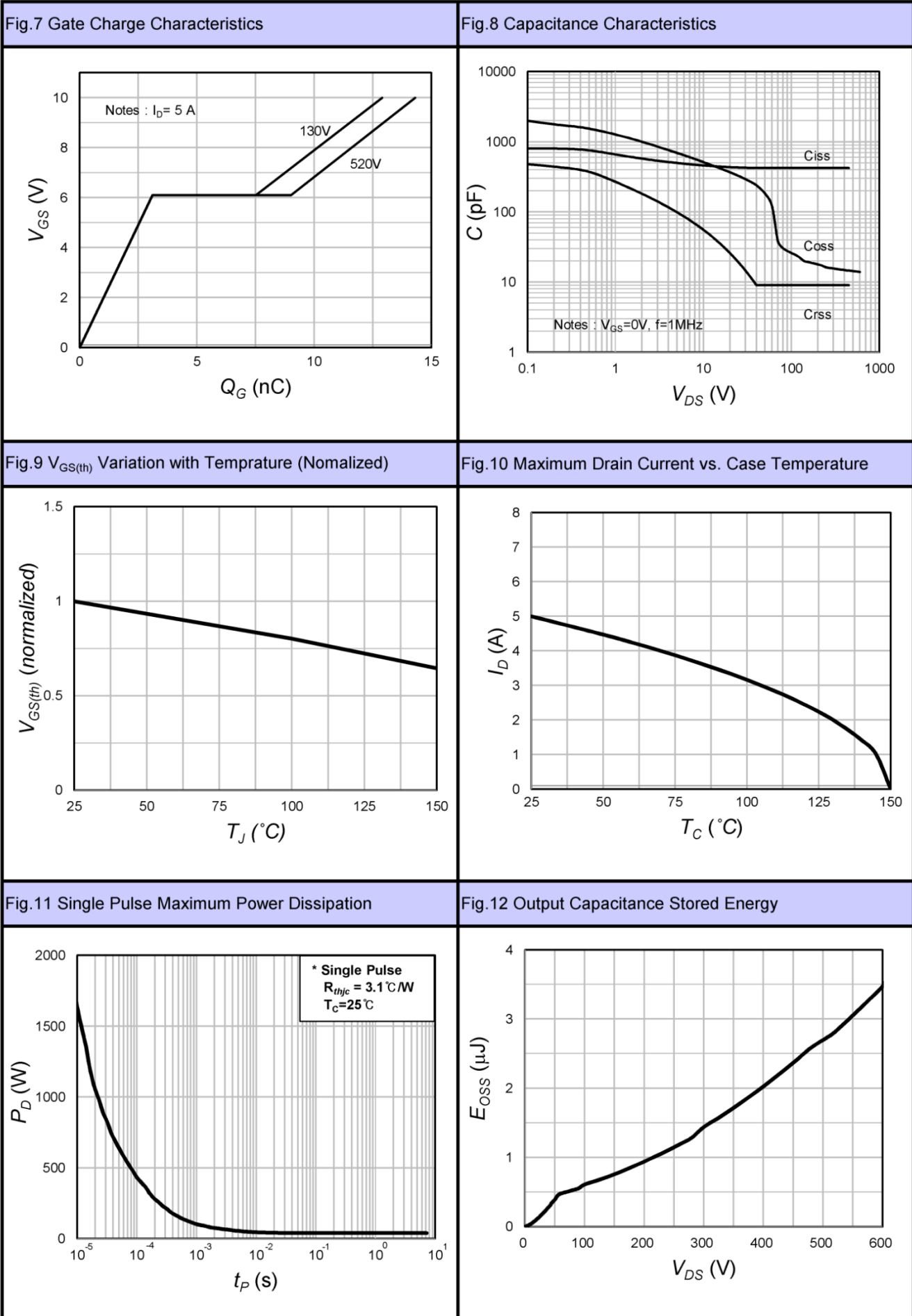
3)  $C_{o(er)}$  is a capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0V to 80%  $V_{(BR)DSS}$

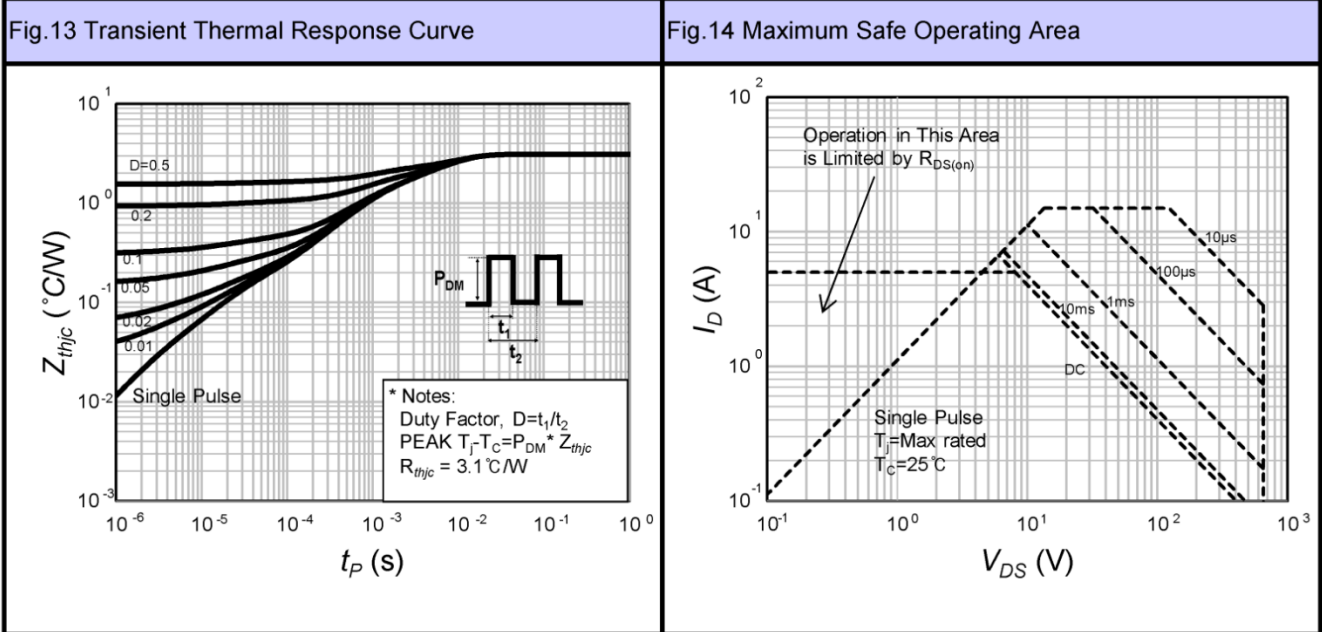
**■ Reverse Diode Characteristics ( $T_c=25^\circ C$  unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Continuous Diode Forward Current	$I_{SD}$	-	-	5.0	A	
Diode Forward Voltage	$V_{SD}$	-	-	1.4	V	$I_{SD} = 5 A, V_{GS} = 0 V$
Reverse Recovery Time	$t_{rr}$	-	315	-	ns	$I_{SD} = 5 A, di/dt = 100 A/\mu s, V_{DD} = 100 V$
Reverse Recovery Charge	$Q_{rr}$	-	2.0	-	$\mu C$	
Reverse Recovery Current	$I_{rrm}$	-	12.5	-	A	

■ Characteristic Graph







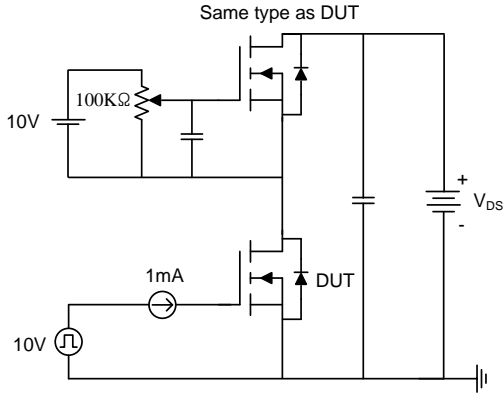
**Test Circuit**


Fig15-1. Gate charge measurement circuit

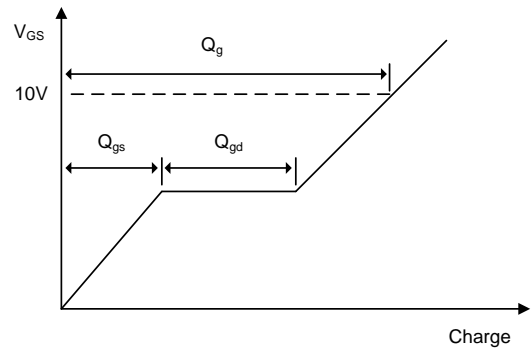


Fig15-2. Gate charge waveform

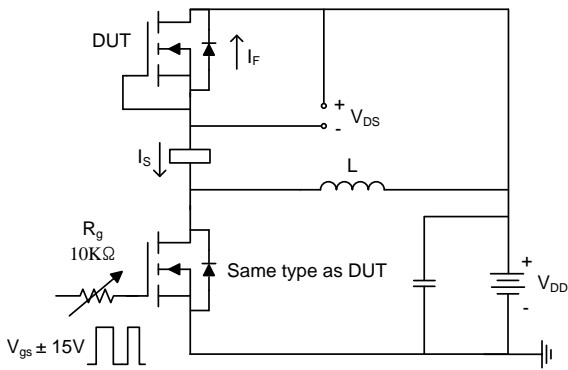


Fig16-1. Diode reverse recovery test circuit

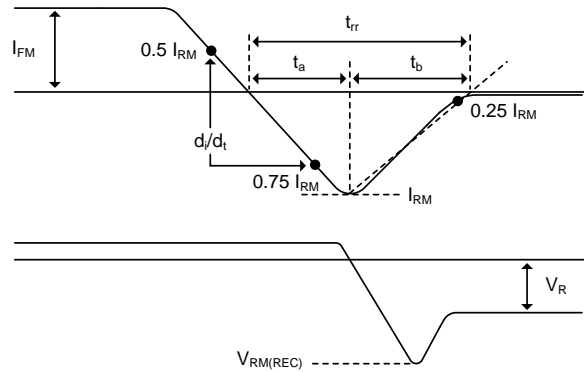


Fig16-1. Diode reverse recovery test waveform

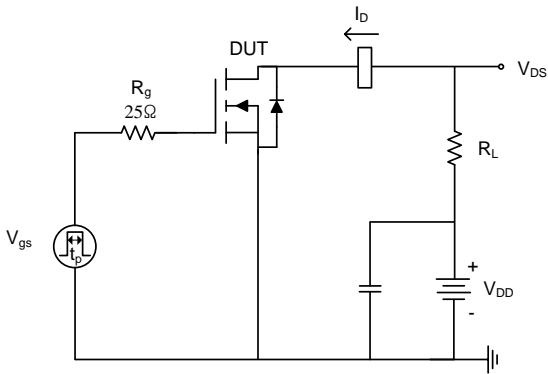


Fig17-1. Switching time test circuit for resistive load

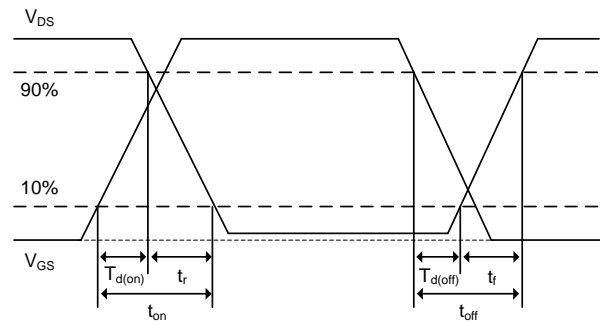


Fig17-2. Switching time waveform

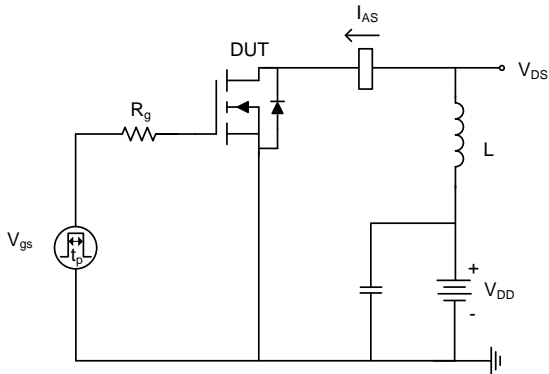


Fig18-1. Unclamped inductive load test circuit

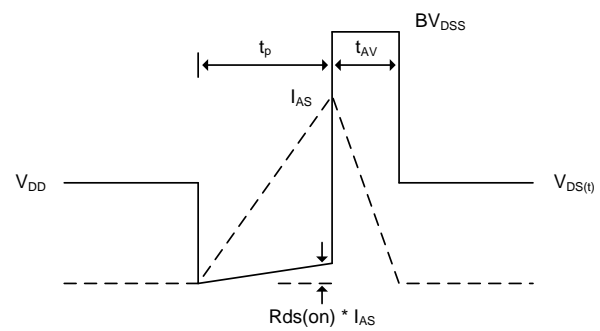
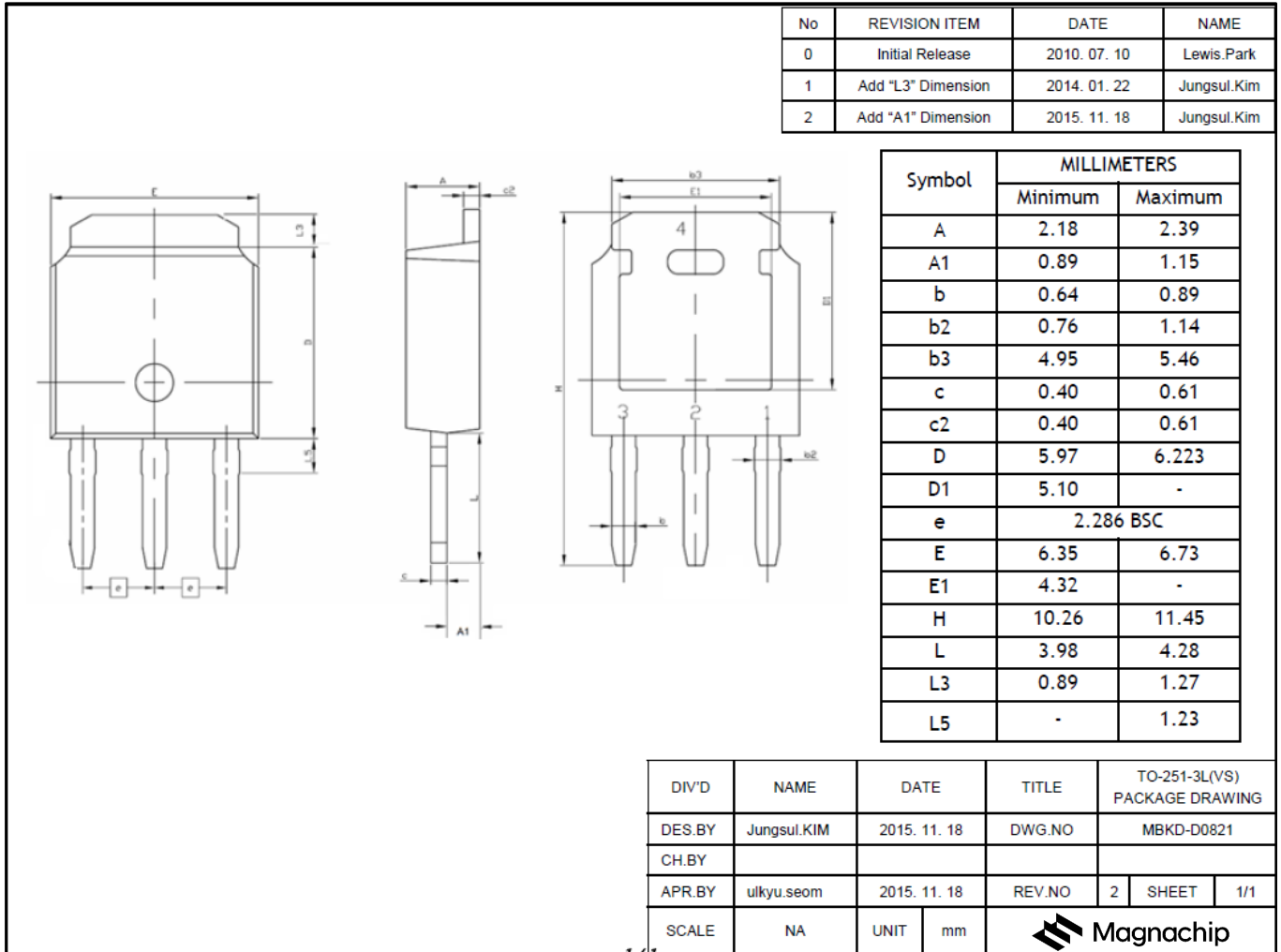


Fig18-2. Unclamped inductive waveform

**■ Physical Dimension**
**TO-251-VS, 3L (IPAK-VS)**


Dimensions are in millimeters, unless otherwise specified





**DISCLAIMER:**

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