MMD70R600Q

700V 0.6Ω N-channel MOSFET

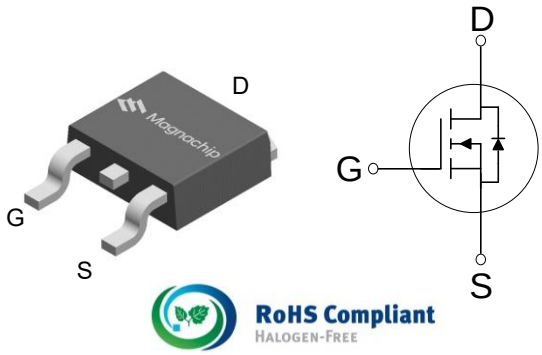
■ Description

MMD70R600Q is power MOSFET using Magnachip's advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI to designers as well as low switching loss.

■ Key Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	750	V
$R_{DS(on),max}$	0.6	Ω
$V_{TH,typ}$	3	V
I_D	7.3	A
$Q_{g,typ}$	15	nC

■ Package & Internal Circuit



■ Features

- Low Power Loss by High Speed Switching and Low On-Resistance
- Excellent ESD robustness
- 100% Avalanche Tested
- Green Package – Pb Free Plating, Halogen Free
- Product validation acc. JEDEC Standard

■ Applications

- PFC Power Supply Stages
- Switching Applications
- Adapter

■ Ordering Information

Order Code	Marking	Temp. Range	Package	Packing	RoHS Status
MMD70R600QRH	70R600Q	-55 ~ 150°C	TO-252(2L)	Reel	Compliant

■ Absolute Maximum Rating (T_c=25°C unless otherwise specified)

Parameter	Symbol	Rating	Unit	Note
Drain – Source voltage	V_{DSS}	700	V	
Gate – Source voltage	V_{GSS}	±30	V	
Continuous drain current	I_D	7.3	A	T_C=25 °C
		4.6	A	T_C=100 °C
Pulsed drain current(1)	I_{DM}	21.9	A	
Power dissipation	P_D	63	W	
Single - pulse avalanche energy	E_{AS}	55	mJ	
MOSFET dv/dt ruggedness	dv/dt	50	V/ns	
Diode dv/dt ruggedness(2)	dv/dt	15	V/ns	
Storage temperature	T_{stg}	-55 ~150	°C	
Maximum operating junction temperature	T_j	150	°C	

1) Pulse width t_P limited by $T_{j,max}$
2) $I_{SD} \leq I_D$, $V_{DS\ peak} \leq V_{(BR)DSS}$

■ Thermal Characteristics

Parameter	Symbol	Value	Unit	Note
Thermal resistance, junction-case max	R_{thjc}	2	°C/W	
Thermal resistance, junction-ambient max	R_{thja}	62.5	°C/W	
Soldering temperature, wavesoldering only allowed at leads(3)	T_{sold}	260	°C	reflow MSL1

3) This parameter can be changed according to internal circumstances

■ Static Characteristics (T_c=25ºC unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain – Source Breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	V_{GS} = 0V, I_D = 0.25mA
Gate Threshold Voltage	$V_{GS(th)}$	2	3	4	V	V_{DS} = V_{GS}, I_D = 0.25mA
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	uA	V_{DS} = 700V, V_{GS} = 0V
Gate Leakage Current	I_{GSS}	-	-	100	nA	V_{GS} = ±30V, V_{DS} = 0V
Drain-Source On State Resistance	$R_{DS(ON)}$	-	0.54	0.6	Ω	V_{GS} = 10V, I_D = 2.1A

■ Dynamic Characteristics (T_c=25ºC unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{iss}	-	539	-	pF	V_{DS} = 100V, V_{GS} = 0V, f = 400kHz
Output Capacitance	C_{oss}	-	20	-		
Reverse Transfer Capacitance	C_{rss}	-	1.1	-		
Effective Output Capacitance Energy Related(4)	$C_{o(er)}$	-	13	-		V_{DS} = 0V to 560V, V_{GS} = 0V, f = 400kHz
Turn On Delay Time	$t_{d(on)}$	-	13	-	ns	V_{GS} = 10V, R_G = 25Ω, V_{DS} = 350V, I_D = 7.3A
Rise Time	t_r	-	29	-		
Turn Off Delay Time	$t_{d(off)}$	-	88	-		
Fall Time	t_f	-	26	-		
Total Gate Charge	Q_g	-	15	-	nC	V_{GS} = 10V, V_{DS} = 560V, I_D = 7.3A
Gate – Source Charge	Q_{gs}	-	4	-		
Gate – Drain Charge	Q_{gd}	-	5.6	-		
Gate Resistance	R_G	-	21	-	Ω	V_{GS} = 0V, f = 1.0MHz

4) $C_{o(er)}$ is a capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0V to 80% $V_{(BR)DSS}$

■ Reverse Diode Characteristics (T_c=25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Continuous Diode Forward Current	I_{SD}	-	-	7.3	A	
Diode Forward Voltage	V_{SD}	-	-	1.4	V	I_{SD} = 7.3A, V_{GS} = 0V
Reverse Recovery Time	t_{rr}	-	298	-	ns	I_{SD} = 7.3A di/dt = 100A/μs V_{DD} = 100V
Reverse Recovery Charge	Q_{rr}	-	2.8	-	μC	
Reverse Recovery Current	I_{rrm}	-	18.6	-	A	

■ Characteristic Graph

Fig.1 Output characteristics.

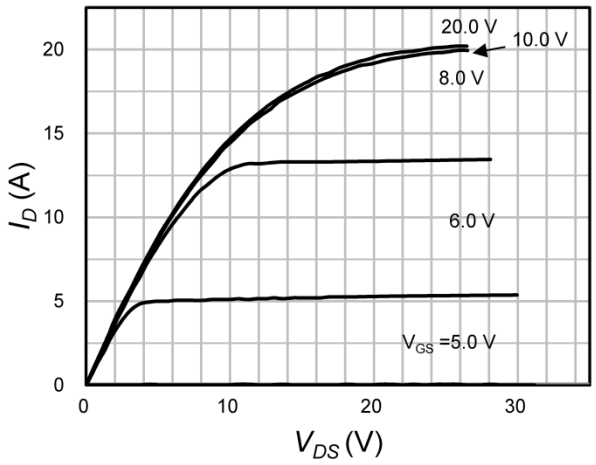


Fig.2 Drain-source on-state resistance vs. drain current

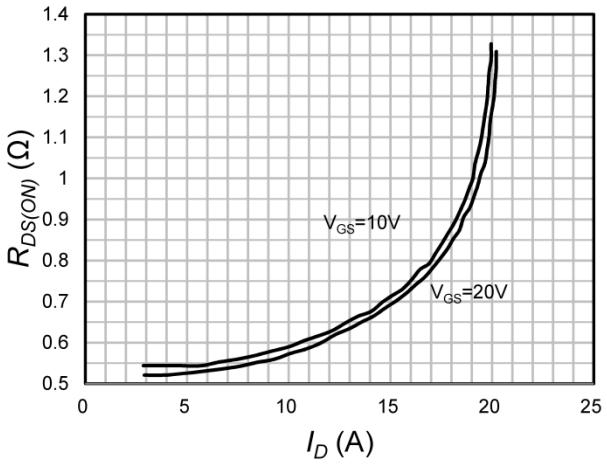


Fig.3 Drain-source on-state resistance (normalized)

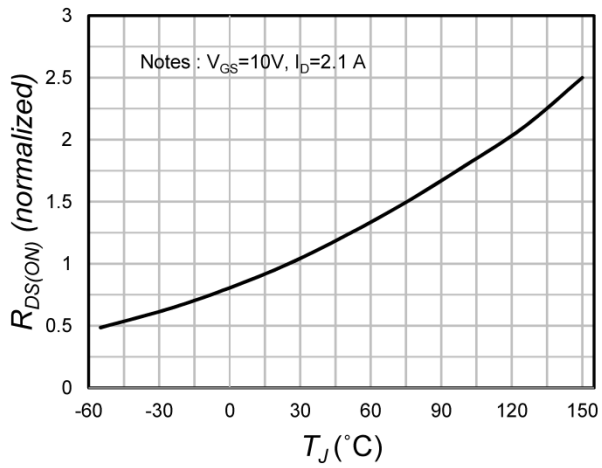


Fig.4 Drain-source breakdown voltage (normalized)

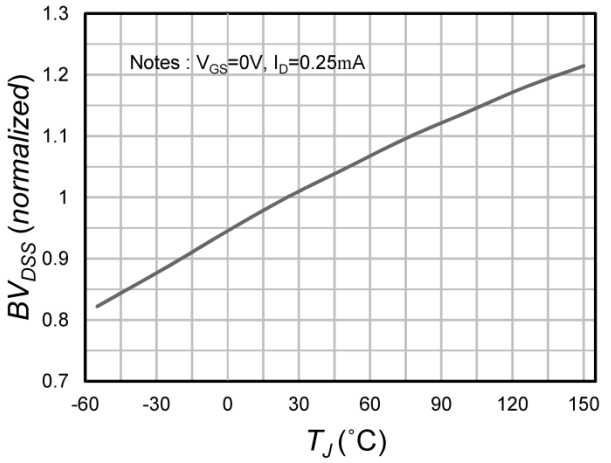


Fig.5 Transfer characteristics

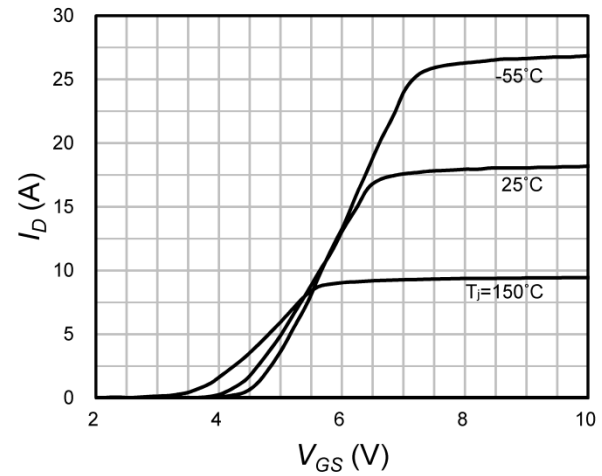


Fig.6 Forward characteristics of reverse diode

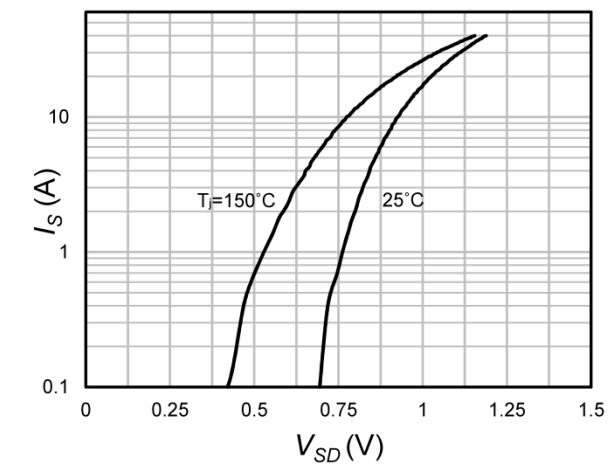


Fig.7 Gate charge

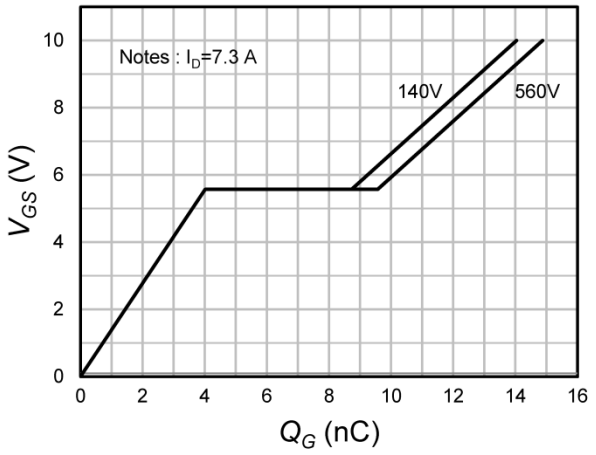


Fig.8 Capacitance characteristics

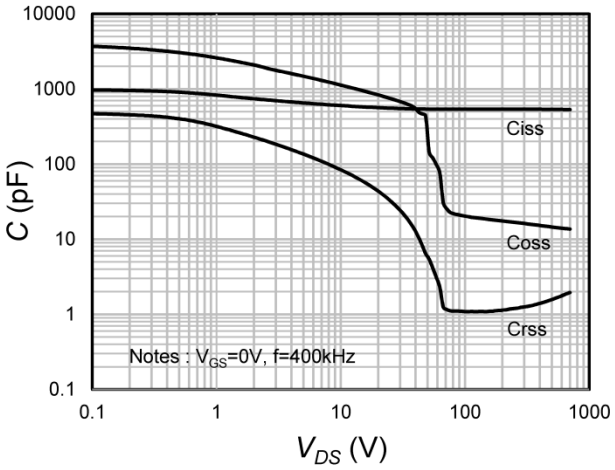


Fig.9 VGS(th) variation vs. temprature (nomalized)

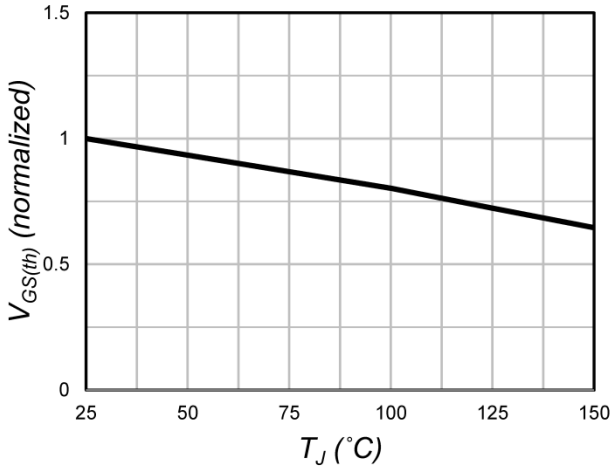


Fig.10 Maximum drain current vs. case temperature

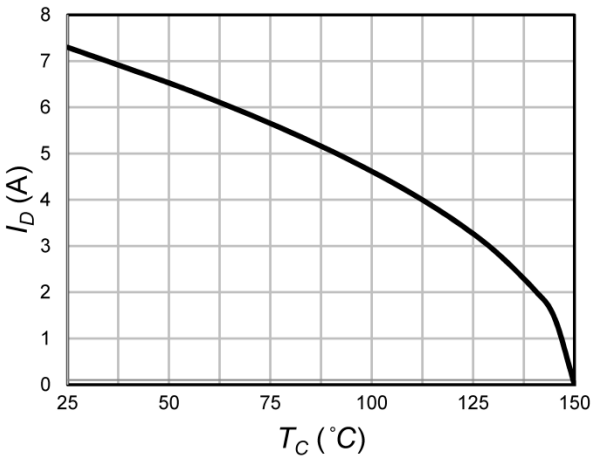


Fig.11 Power dissipation

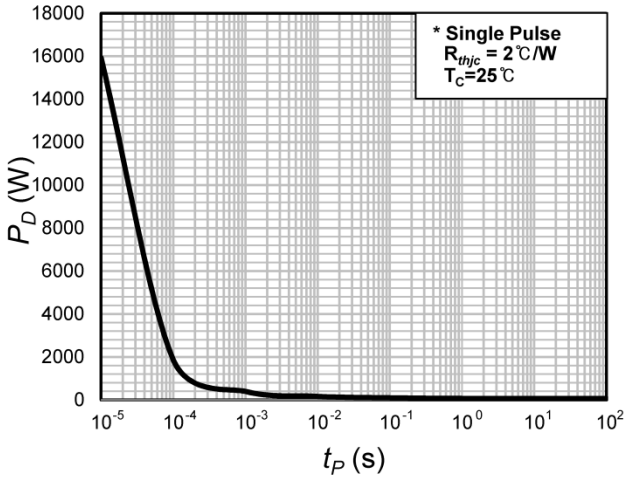


Fig.12 Output capacitance stored energy

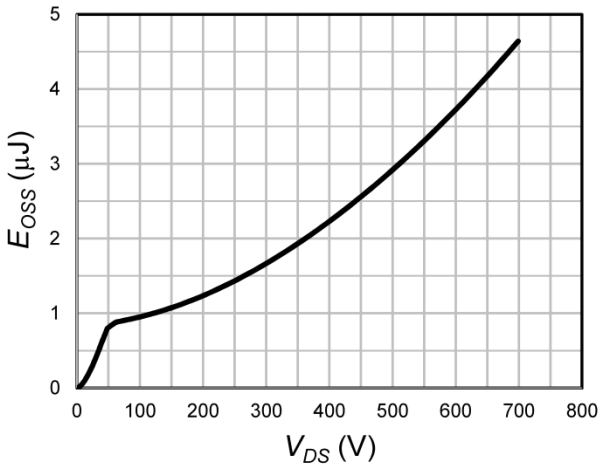


Fig.13 Transient thermal impedance

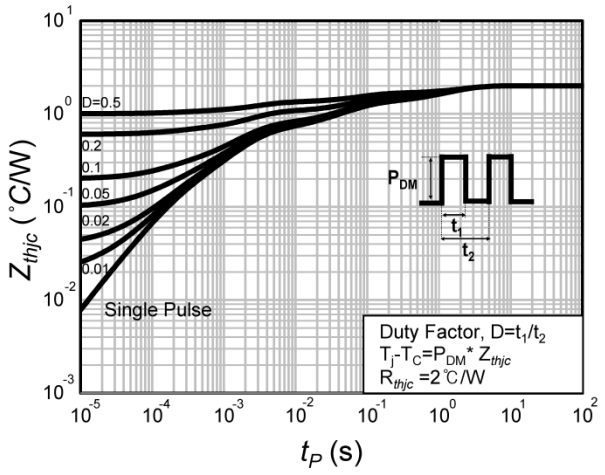
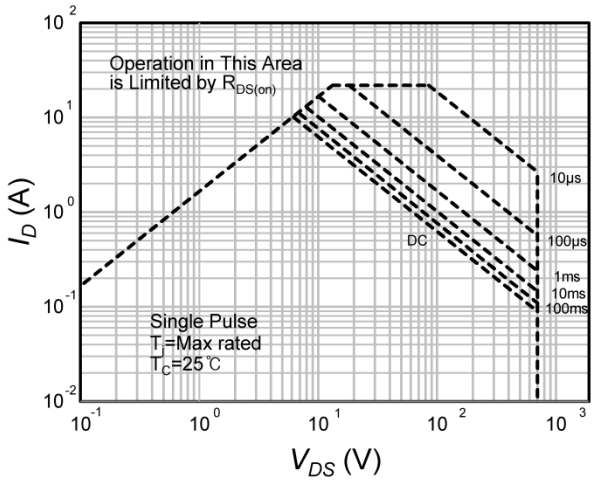


Fig.14 Safe operating area



■ Test Circuit

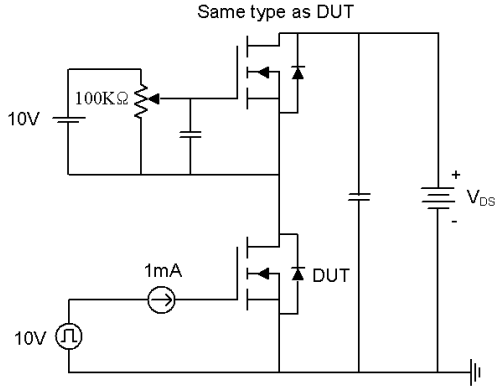


Fig15-1. Gate charge measurement circuit

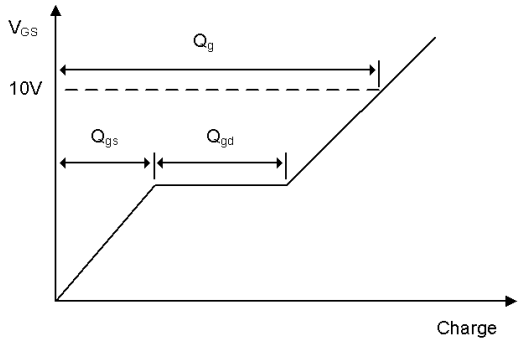


Fig15-2. Gate charge waveform

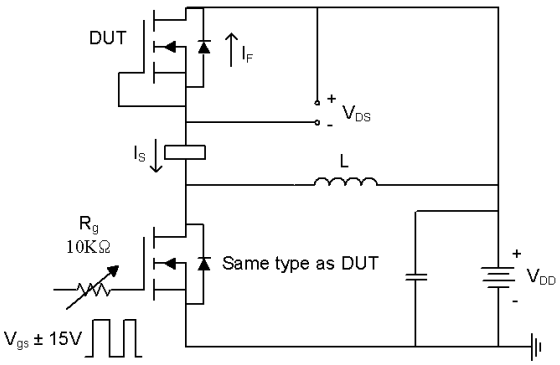


Fig16-1. Diode reverse recovery test circuit

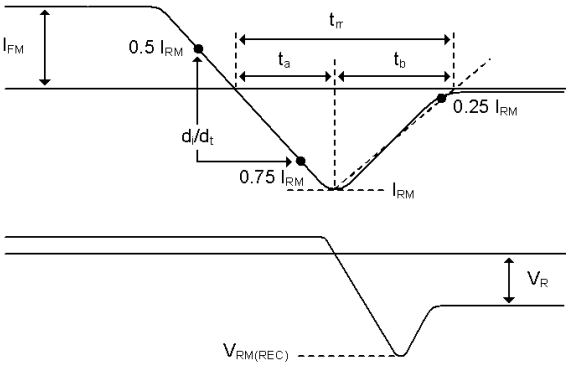


Fig16-2. Diode reverse recovery test waveform

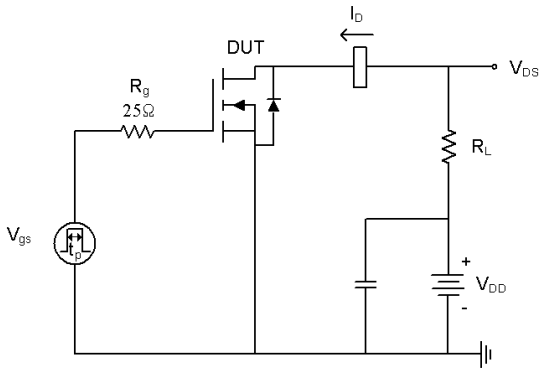


Fig17-1. Switching time test circuit for resistive load

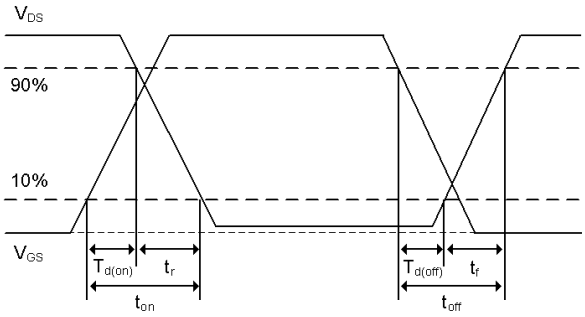


Fig17-2. Switching time waveform

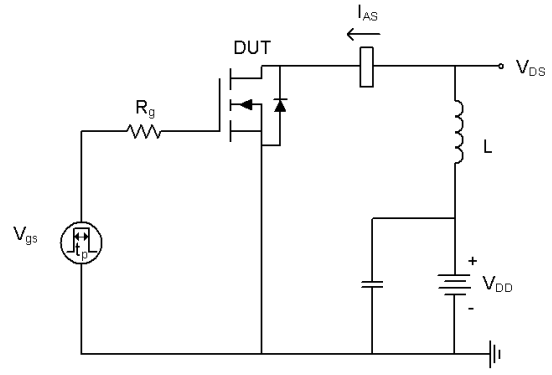


Fig18-1. Unclamped inductive load test circuit

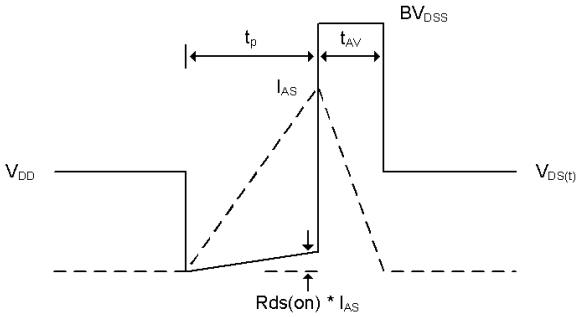
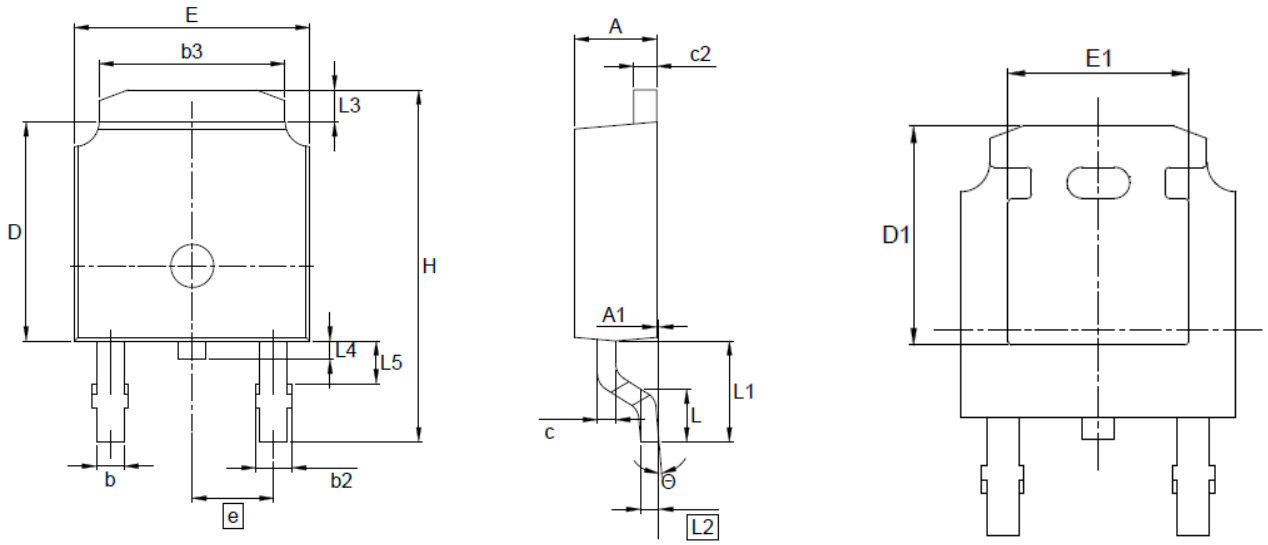


Fig18-2. Unclamped inductive waveform

■ Physical Dimension

TO-252 (2L)



Symbol	Dimension (mm)		
	Min	Nom	Max
E	6.35	–	6.73
L	1.40	1.52	1.78
L1		2.74 REF	
L2		0.508 BSC	
L3	0.89	–	1.27
L4	–	–	1.02
L5	–	–	1.52
D	5.97	6.10	6.22
H	9.40	–	10.41
b	0.64	–	0.89
b2	0.76	–	1.14
b3	4.95	–	5.46
e		2.286 BSC	
A	2.18	–	2.39
A1	–	–	0.13
c	0.46	–	0.61
c2	0.46	–	0.89
D1	5.21	–	–
E1	4.32	–	–
Θ	0°	–	10°

Note : Package body size, length and width do not include mold flash, protrusions and gate burrs.

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