



MDY10N025RH

Single N-channel Trench MOSFET 100V 2.5mΩ 240A

General description

MDY10N025RH uses advanced Magnachip's MV MOSFET Technologies, which provides high performance in on-state resistance, fast switching, parallel performance and excellent quality.

MDY10N025RH is the best solution for high power application where thermal behavior.

Driver source pin avoids gate ringing and false triggering which would normally require switching loss to be limited to manage the source stray inductance of normal package.

M2PAK-7P



Top View

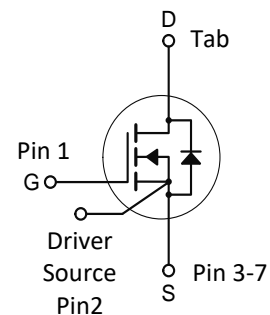
Bottom View

Features and benefits

- Very low on-resistance $R_{DS(on)}$
- 100% Avalanche / R_g / ΔV_{DS} Tested
- High Reliability Package Solution

Applications

- Motor Inverter
- Battery Management
- Power Inverter



Key performance parameters

V_{DS}	100	V
$R_{DS(on), max}$	0.0025	Ω
I_D	240	A
Q_G	167	nC
Junction temperature, $_{max}$	175	$^{\circ}C$



Ordering information

Type / Ordering Code	Package	Marking	Packing	RoHS Status
MDY10N025RH	M2PAK-7P	10N025	Tape & Reel	Halogen Free

<http://www.magnachip.com/powersolutions>



Maximum ratings, at $T_J = 25^\circ\text{C}$, unless otherwise specified

Parameter		Symbol	Rating	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain current	$T_C=25^\circ\text{C}$ Silicon Limited	I_D	306	A
	$T_C=25^\circ\text{C}$ Package Limited		240	A
	$T_C=100^\circ\text{C}$ Silicon Limited		217	A
¹⁾ Pulsed drain current	$T_C=25^\circ\text{C}$	I_{DM}	960	A
Total power dissipation	$T_C=25^\circ\text{C}$	P_{tot}	469	W
	$T_C=100^\circ\text{C}$		234	W
²⁾ Avalanche energy, single pulse		E_{AS}	613	mJ
Operating and storage temperature		T_j, T_{stg}	- 55 ~ 175	$^\circ\text{C}$

Thermal characteristics

Parameter		Symbol	Rating	Unit
Thermal resistance, junction - case		$R_{\theta JC}$	0.32	$^\circ\text{C/W}$
³⁾ Thermal resistance, junction - ambient		$R_{\theta JA}$	30	$^\circ\text{C/W}$

Notes

- Pulse width limited by T_{jmax}
- E_{AS} is tested at starting $T_j = 25^\circ\text{C}$, $L = 1.0\text{mH}$, $I_{AS} = 35\text{A}$, $V_{DD} = 50\text{V}$, $V_{GS} = 10\text{V}$
- Surface mounted FR-4 board by JEDEC (jesd51-7)

Electrical Characteristics ($T_J = 25^\circ\text{C}$)

Static characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=250\ \mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	2.0	2.8	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\ \mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.2	2.5	m Ω	$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$
Gate resistance	R_G	-	3.0	-	Ω	f=1MHz
Transconductance	g_{fs}	-	120	-	S	$V_{DS}=10\text{ V}$, $I_D=100\text{ A}$

Dynamic characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Input capacitance	C_{iss}	-	12508	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, f=1 MHz
Output capacitance	C_{oss}	-	1457	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	14	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	33	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=3\Omega$
Rise time	t_r	-	21	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=3\Omega$
Turn-off delay time	$t_{d(off)}$	-	137	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=3\Omega$
Fall time	t_f	-	43	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=3\Omega$

Gate charge characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Gate to source charge	Q_{gs}	-	45	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{gs(th)}$	-	39	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	37	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	43	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	167	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.3	-	V	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$

Source-drain diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Diode continuous forward current	I_S	-	-	240	A	-
Diode pulse current	$I_{S,pulse}$	-	-	960	A	pulsed; $t_p \leq 10\ \mu\text{s}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}$, $I_F=100\text{ A}$
Reverse recovery time	t_{rr}	-	117	-	ns	$I_F=100\text{ A}$, $d_I/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	408	-	nC	$I_F=100\text{ A}$, $d_I/dt=100\text{ A}/\mu\text{s}$

Electrical characteristics diagrams

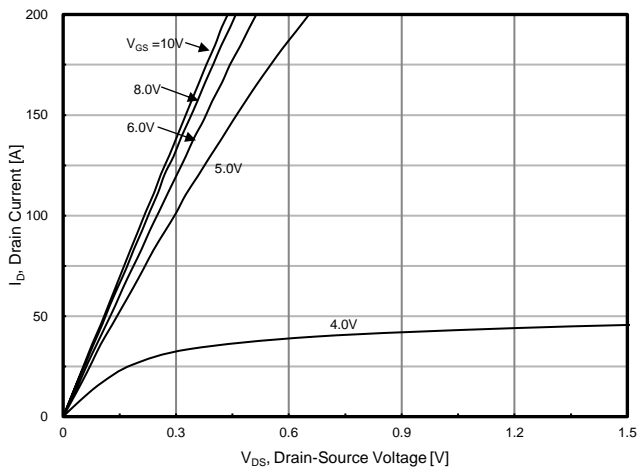


Fig. 1. Output Characteristics

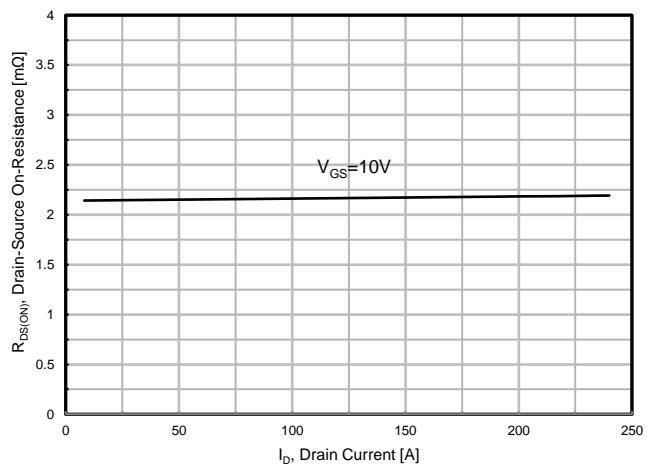


Fig. 2. Static On-Resistance Variation

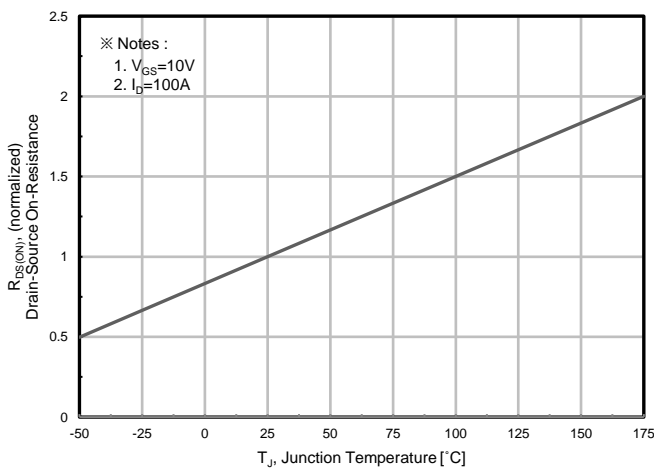


Fig. 3. On-Resistance vs. Junction Temperature

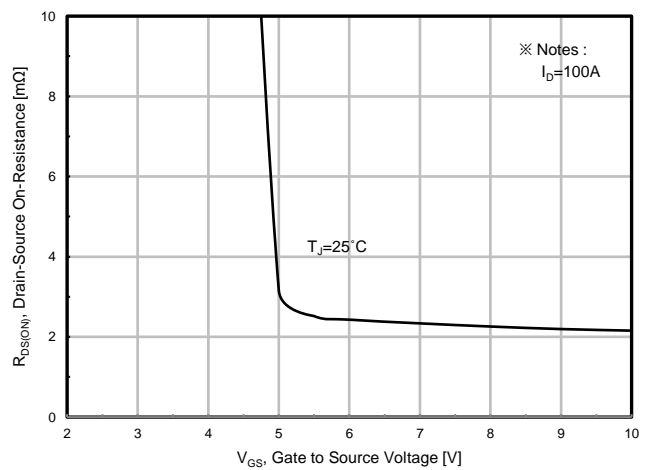


Fig. 4. On-Resistance vs. Gate to Source Voltage

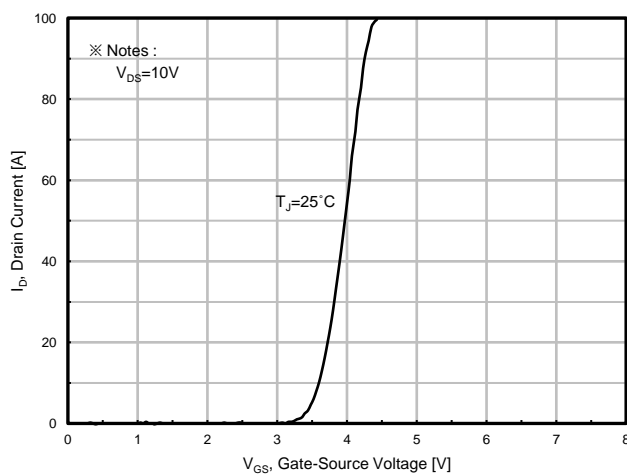


Fig. 5. Transfer Characteristics

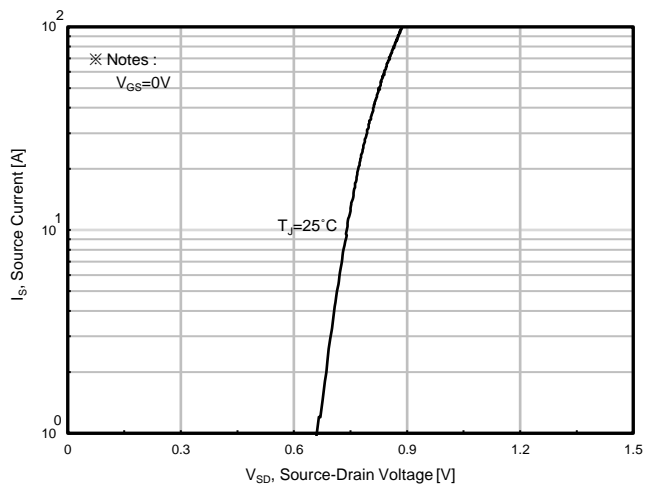


Fig. 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Electrical characteristics diagrams

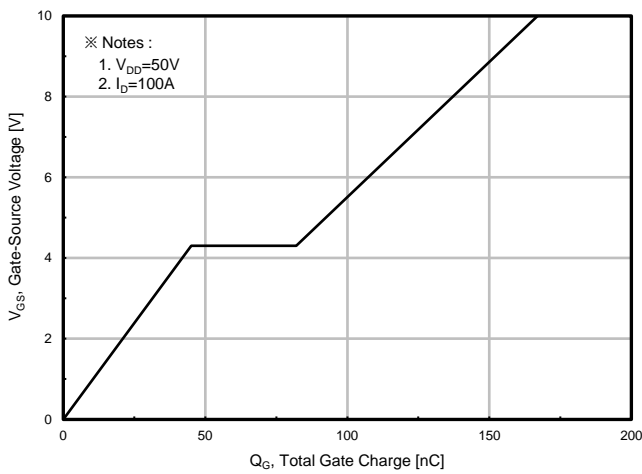


Fig. 7. Gate Charge

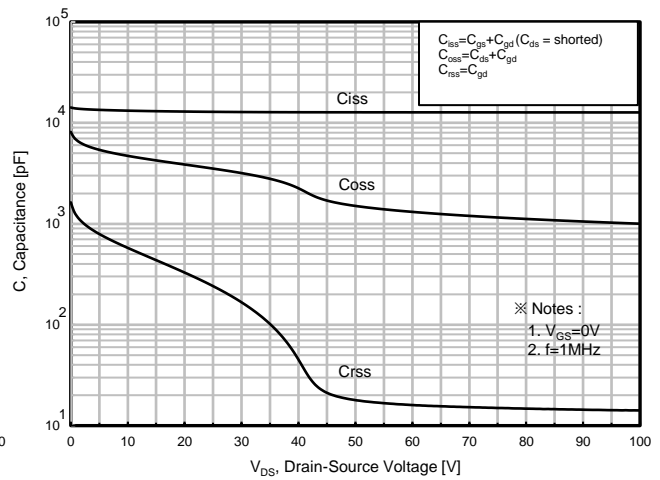


Fig. 8. Capacitances

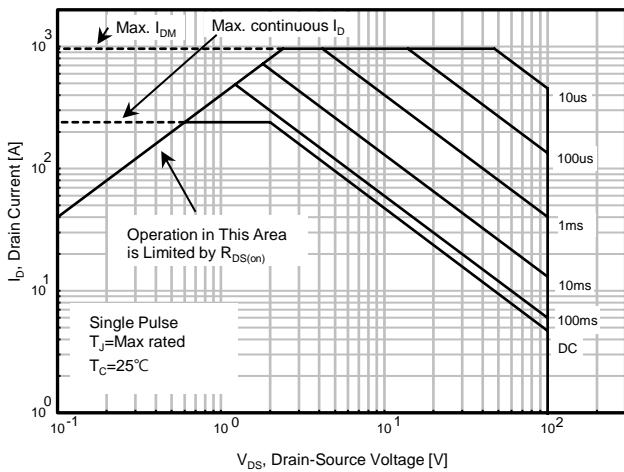


Fig. 9. Safe Operating Area

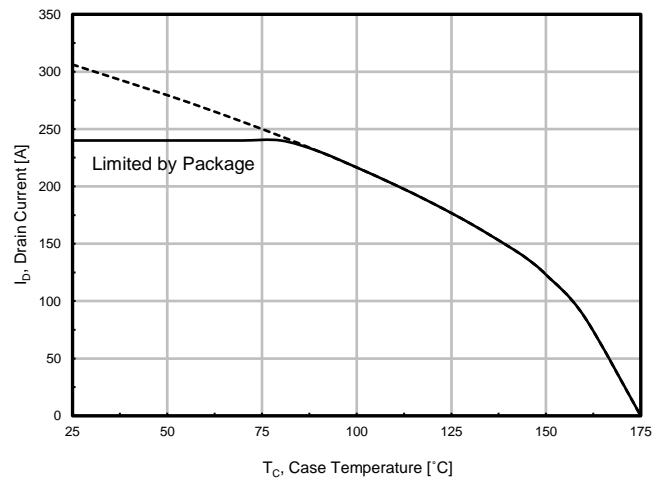


Fig. 10. Maximum Drain Current vs. Case Temperature

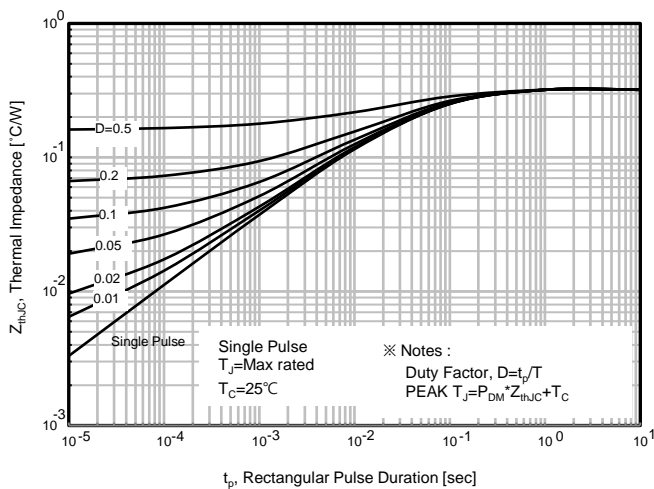
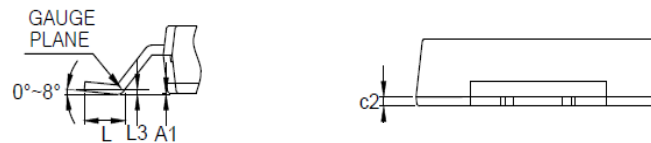
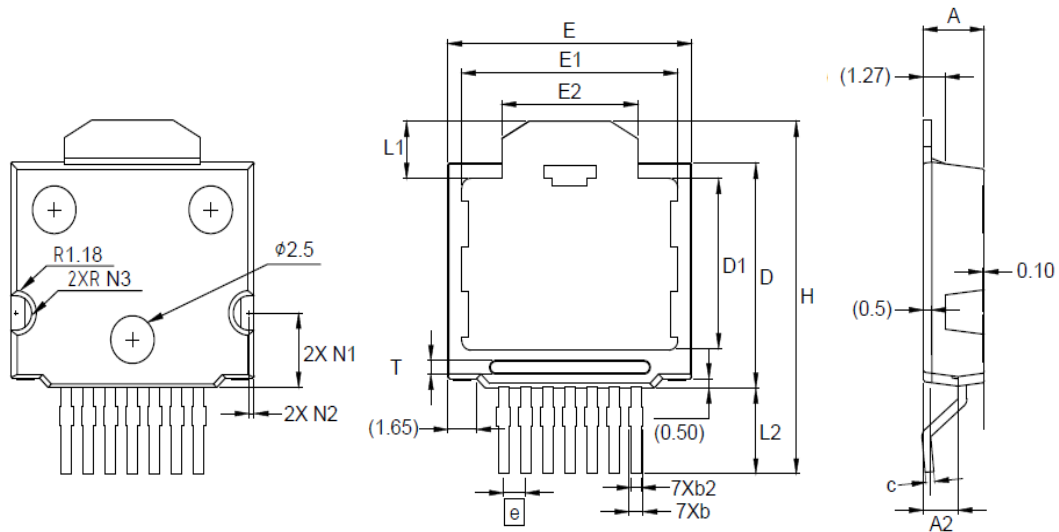


Fig. 11. Transient Thermal Impedance

Package information

M2PAK-7P




Symbol	Dimension (mm)		
	Min	Nom	Max
A	3,40	-	3,60
A1	0,00	-	0,25
A2	1,80	-	2,20
b	0,50	-	0,70
b2	0,50	-	1,00
c	0,40	-	0,60
c2	0,40	-	0,60
D	11,70	-	11,90
D1	8,90	-	9,10
E	13,90	-	14,10
E1	12,30	-	12,50
E2	7,75	-	7,85
T	0,60		0,70
e	BSC 1,27		
H	18,00	-	19,00
L	2,22	-	2,42
L1	2,90	-	3,10
L2	4,35	-	4,65
L3	BSC 0,25		
N1	3,80	-	4,00
N2	0,25	-	0,35
N3	0,80	-	1,00

Note : Package body size, length and width do not include mold flash, protrusions and gate burrs.

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