MagnaChip

# MSI6000

## 11-Channel Level Shifter with Gate Voltage Shaping and Discharge Functions



## General Description

The MSI6000 is a level shifter IC with 11-channel intended for use in LCD Display application such as Note-book.

The device converts signal from logic-level generated by T-CON to the high voltage level used by the display panel.

6 channels Level shifter support gate voltage Shaping, which can be used to improve picture quality by reducing image sticking.

## Features

- 11-Channel level shifter support 6 x GLK, VST, BRST, DSCH, DRST, and EVEN Signals
- VGH level up to 37.5V
- VGL Level down to -15V
- Panel DISCHARGE Function
- Suitable for 6-Phase Applications
- Gate Voltage Shaping on Channels 1 to 6 channels
- 24-Pin 4x4 mm QFN Package

## Application

- LCD Note-Book Panels

## Operational Diagram

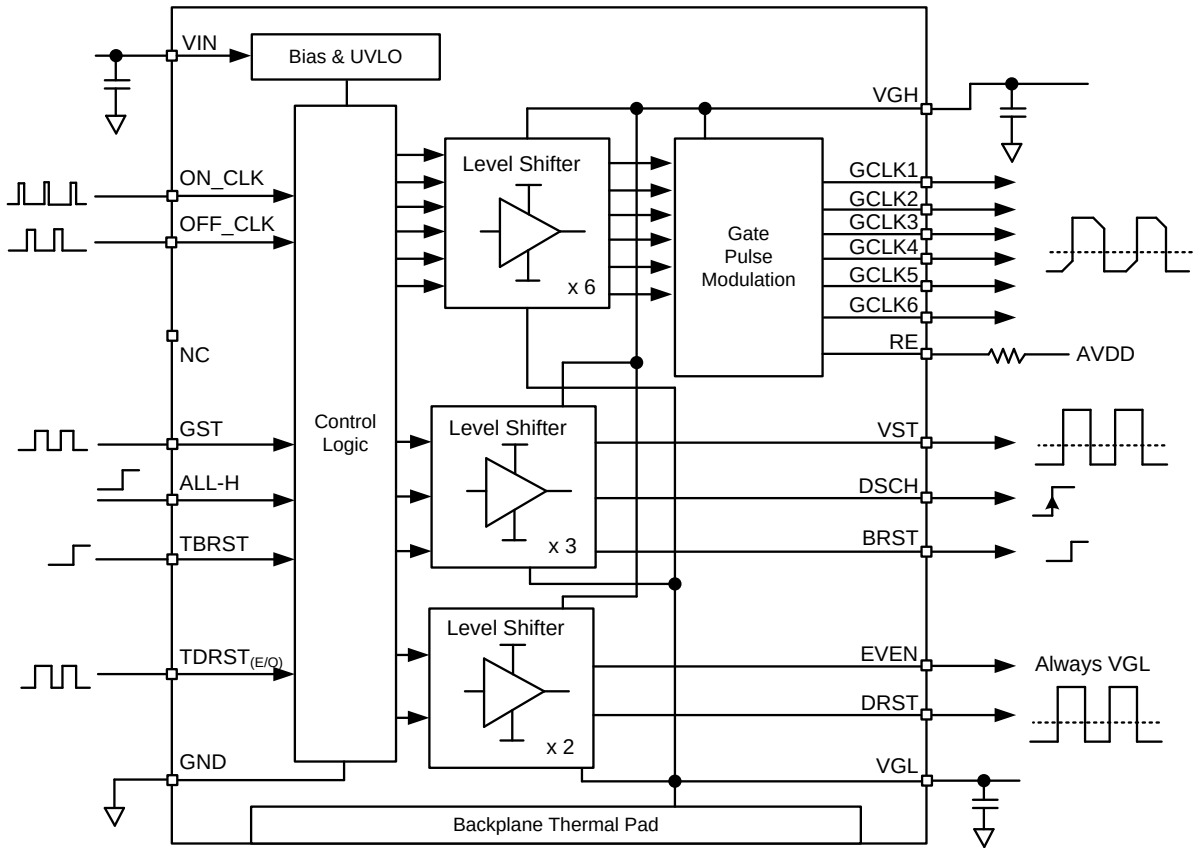
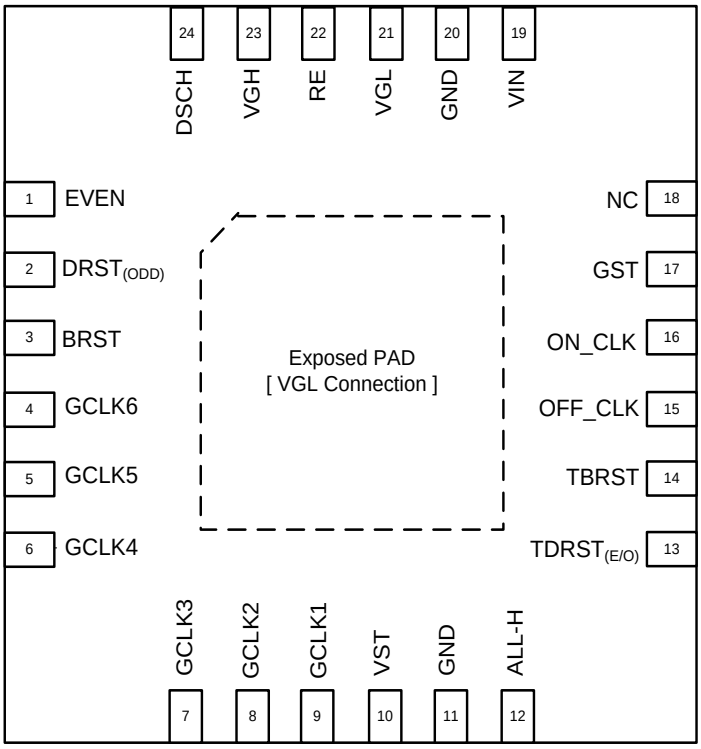



**Figure 1) Block Diagram**

## Bill of Materials

| item | Part Number | Manufacturer | Description | Qty. |
|---|---|---|---|---|
| IC | MSI6000 | Magnachip | 11 channel Level shifter | 1 |
| $C_{IN}$ | CL10B105KO8NNNC | Samsung | 1uF, 16V, 1608, X7R | 1 |
| $C_{VGH}$ / $C_{VGL}$ | CL21B105KBFNNNF | Samsung | 1uF, 50V, 2012, X7R | 2 |

## Pin Configuration



## Pin Definitions

| Pin# | Name | IO | Description |
|---|---|---|---|
| 1 | EVEN | O | **Level shifter Output**, Always VGL Output Pin. |
| 2 | DRST(ODD) | O | **Level shifter Output**, High voltage level shifter output |
| 3 | BRST | O | **Level shifter Output** |
| 4 | GLK6 | O | **Level Shifter Outputs.** High voltage level shifter outputs. |
| 5 | GLK5 | O | **Level Shifter Outputs.** High voltage level shifter outputs. |
| 6 | GLK4 | O | **Level Shifter Outputs.** High voltage level shifter outputs. |
| 7 | GLK3 | O | **Level Shifter Outputs.** High voltage level shifter outputs. |
| 8 | GLK2 | O | **Level Shifter Outputs.** High voltage level shifter outputs. |
| 9 | GLK1 | O | **Level Shifter Outputs.** High voltage level shifter outputs. |
| 10 | VST | O | **Level shifter Output for Vertical Start** |
| 11 | GND | G | **Level shifter Ground** |
| 12 | ALL_H | I | Discharging Input |
| 13 | TDRST(E/O) | I | **Level shifter Input for Gate DRST** |
| 14 | TBRST | I | **Level shifter Input BRST** |
| 15 | OFF_CLK | I | **Level shifter Input for GPM Start and GPM Duty**, High voltage level shifter logic input |
| 16 | ON_CLK | I | **Level shifter Input for GPM Start and GPM Duty**, High voltage level shifter logic input |
| 17 | GST | I | **Level shifter Input for Gate Start**, Synchronized with VST |
| 18 | NC | I | **Not Connected** |
| 19 | VIN | P | **VIN Input Supply Voltage** |
| 20 | GND | G | **Level shifter Ground** |
| 21 | VGL | I | **Negative Supply for Level Shifter.** VGL supplies negative power to level shifter for Gate-Off. Place ceramic capacitor of sufficient capacity considering current level needed. Shunt capacitor to GND as close as possible to this pin. |
| 22 | RE | I | **Gate High Output Fall Time and Gate Low Output rise time Setting pin**. Connect a resistor to VDD to set the transition slope |
| 23 | VGH | I | **Positive Supply for Level Shifter.** VGH supplies positive power to ODD for Gate-On. Place ceramic capacitor of sufficient capacity considering current level needed. Shunt capacitor to GND as close as possible to this pin. |
| 24 | DSCH | O | **Output for Discharge**. Negated high voltage level-shifted output |
| N/A | E-PAD | G | Connect VGL |

## Absolute Maximum Ratings

Absolute Maximum ratings [ $T_A$=25℃, Unless otherwise noted ]

| Parameter | Value | Unit |
|---|---|---|
| ON_CLK, OFF_CLK, GST, TDRST, ALL-H to GND | -0.3 to 6.0 | V |
| VGH, RE to GND | -0.3 to 39.0 | V |
| DSCH, CLK1~6, ODD, BRST, VST, VGH to VGL | -0.3 to 54.0 | V |
| VGL, EVEN to GND | -15.0 to +0.3 | V |
| Power Dissipation, PD @ $T_A$=70℃ (1) | 2 (Max.) | W |
| Package Thermal Resistance ($\theta_{JA}$) | 40 (Max.) | ℃/W |
| Operating ambient temperature range (2) | -25 to +85 | ℃ |
| Operating Junction temperature range (2) | -25 to +125 | ℃ |
| Ambient Storage Temperature | -65 to +150 | ℃ |
| ESD HBM Rating | 2 | kV |
| ESD MM Rating | 200 | V |
| ESD CDM Rating | 700 | V |

Note :

1) Highly depends on the PCB heat dissipation. Tester with the Thermal Characteristics the condition below $T_A$=70℃
2) Measured in still air-free convection condition(conforms to EIA/JESD51-2) on high effective thermal conductivity JESD51-7 test board.

## Electrical Characteristics

$V_{IN}$=3.3V, $V_{GH}$ = 20V, $V_{GL}$ = -8.5V : $T_A$=-25℃ to +85℃, Typical values are at $T_A$=25℃(unless otherwise noted.)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General Section** | | | | | | |
| $V_{IN}$ | Input Voltage Range | | 2.2 | 3.3 | 5.0 | V |
| $I_Q$ | Quiescent Current | LS Input =GND, No Load | | 0.01 | 1 | mA |
| $I_{GH}$ | VGH Supply Current | LS Input =GND, No Load | | 1 | 2 | mA |
| $I_{GL}$ | VGL Supply Current | LS Input =GND, No Load | | 0.3 | 0.5 | mA |
| $V_{IN\_UVLO\_H}$ | $V_{IN}$ UVLO Rising Threshold | | | 2.0 | | V |
| $T_{LIMIT}$ | Thermal Shutdown(Note1) | | | 150 | | ℃ |
| $T_{HYST}$ | Thermal Shutdown Hysteresis(Note1) | | | 30 | | ℃ |
| **Level Shifter** | | | | | | |
| $V_{GH}$ | $V_{GH}$ Input Voltage Range | $V_{IN}$=3.3V | 5 | 20 | 37.5 | V |
| $V_{GL}$ | $V_{GL}$ Input Voltage Range | $V_{IN}$=3.3V | -15 | -8.5 | -5 | V |
| $V_{GH}$-$V_{GL}$ | $V_{GH}$ to $V_{GL}$ Voltage Range(Note1) | $V_{IN}$=3.3V | 10 | | 53 | V |
| $V_{OH}$ | Output High Voltage | $I_H$=-10mA | $V_{GH}$-1 | | | V |
| $V_{OL}$ | Output Low Voltage | $I_H$=+10mA | | | $V_{GL}$+1 | V |
| $V_{GH\_UVLO\_H}$ | $V_{GH}$ UVLO Rising Threshold | | | 4 | | V |
| $V_{GH\_UVLO\_H}$ | $V_{GH}$ UVLO Falling Threshold | | | 3 | | V |
| $t_{PH}$ | Propagation Rising Delay | $C_{LOAD}$=100pF, 50% to 50% | | 100 | 200 | ns |
| $t_{PL}$ | Propagation Falling Delay | $C_{LOAD}$=100pF, 50% to 50% | | 150 | 300 | ns |
| $t_R$ | Rising time | $C_{LOAD}$=100pF, 10% to 90% | | 10 | 70 | ns |
| $t_F$ | Falling time | $C_{LOAD}$=100pF, 90% to 10% | | 15 | 70 | ns |
| $t_{in\_min}$ | Minimum On time(Note1) | | 100 | | | ns |
| $f_{MAX}$ | Maximum Operating Frequency(Note1) | $C_{LOAD}$=100pF | | | 200 | kHz |
| $R_{RE}$ | RE Resistance(Note1) | | | 300 | | Ω |
| ROH | CLK1~6 Output Impedance | $I_{OH}$=-10mA | | 12 | | Ω |
| ROL | CLK1~6 Output Impedance | $I_{OH}$=+10mA | | 7 | | Ω |
| ROH | ODD, DSCH, VGH, BRST Output Impedance | $I_{OH}$=-10mA | | 35 | | Ω |
| ROL | ODD, DSCH, VGH, BRST Output Impedance | $I_{OH}$=+10mA | | 16 | | Ω |
| **Discharging** | | | | | | |
| $V_{DIS}$ | Enable Start (Note1) | ALL-H Falling | | 1.8 | | V |
| $V_{ALL\_H\_IH}$ | ALL_H High Level Input Voltage | | 1.4 | | | V |
| $V_{ALL\_H\_IL}$ | ALL_H Low Level Input Voltage | | | | 0.6 | V |
| **Logic Input (GST, ONCLK, OFFCLK, TDRST)** | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | 1.4 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.6 | V |
| $I_{IL}$ | Input Leakage Current | ON_CLK=OFF_CLK=0V | -1 | | 1 | uA |

Note1) Guaranteed by design, characterization and correlation with process controls, Not fully tested in production

## Level shifters

The MSI6000 has the 11-channel high voltage level shifter. It is designed to shift the level of a logic signal to VGH or VGL. VGH is positive supplies with voltage range for +5V to +37.5V. and VGL is the negative supply with voltage range for -15V to -5V.

Figure 2 contains a simplified block diagram of one channel with gate voltage shaping.

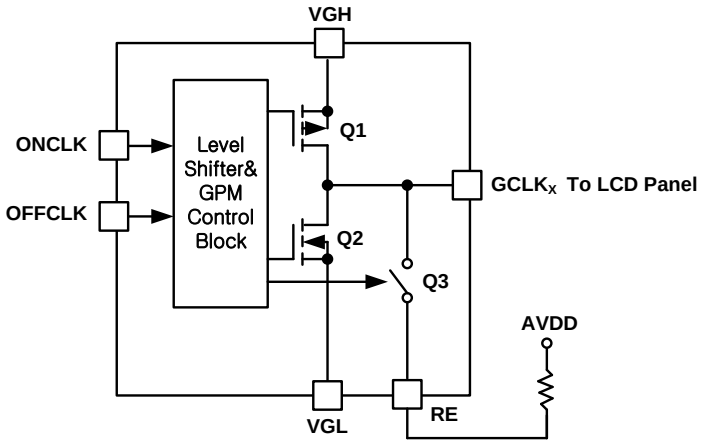



**Figure 2) Level shifter Channel with Gate Voltage Shaping**

On the rising edge of ONCLK, Q1 turns on, Q2 turns off and Q3 is turned on during a certain time which is set by the RE resistor. So GCLK1 is charged by AVDD voltage through the RE resistor. After that, Q3 is turned off and Q1 is turned on and GCLK1 voltage goes up to VGH. On the rising edge of OFFCLK, Q1 turns off, Q3 is turned on, and GCLK1 voltage slices through Q3 and the RE resistor is connected to RE pin. On the falling edge of OFFCLK, Q2 is turned on and Q3 is turned off, and GCLK1 voltage is driven to VGL.

This sequence is shown in the below figure.

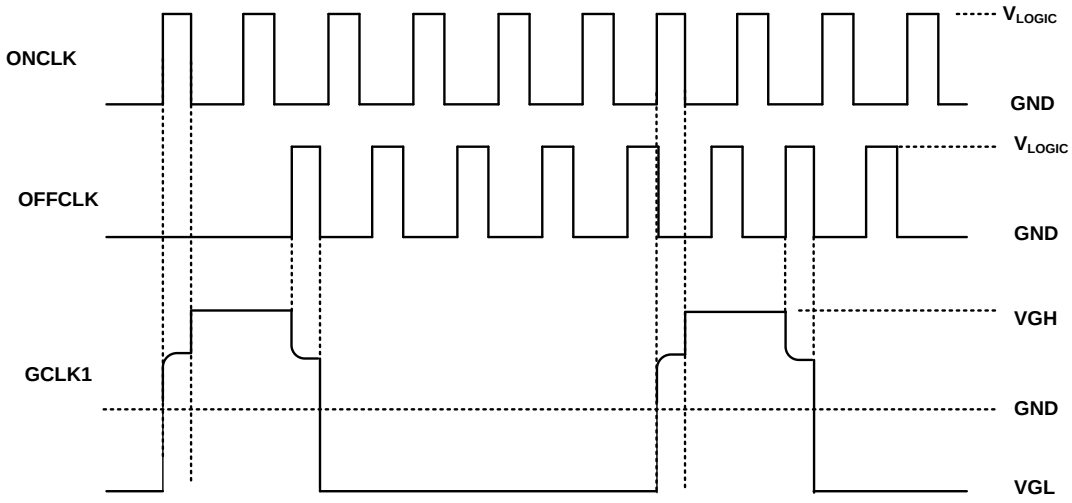



**Figure 3) Gate Voltage Shaping Timing Diagram**

## Power Sequence

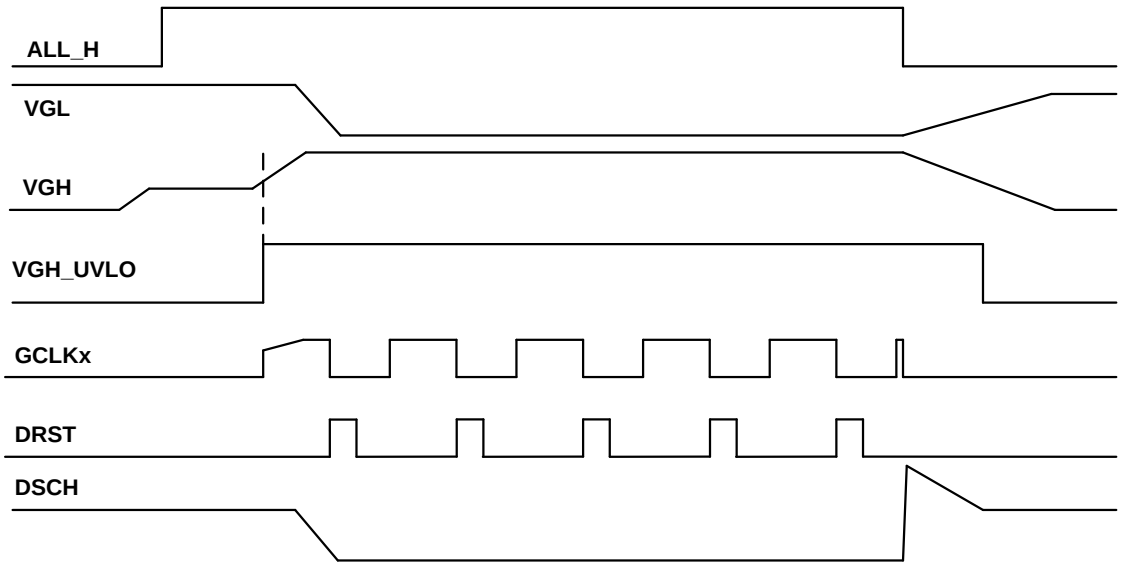



**Figure 4 ) Power Sequence**

## Level shifter Input / Output Waveform

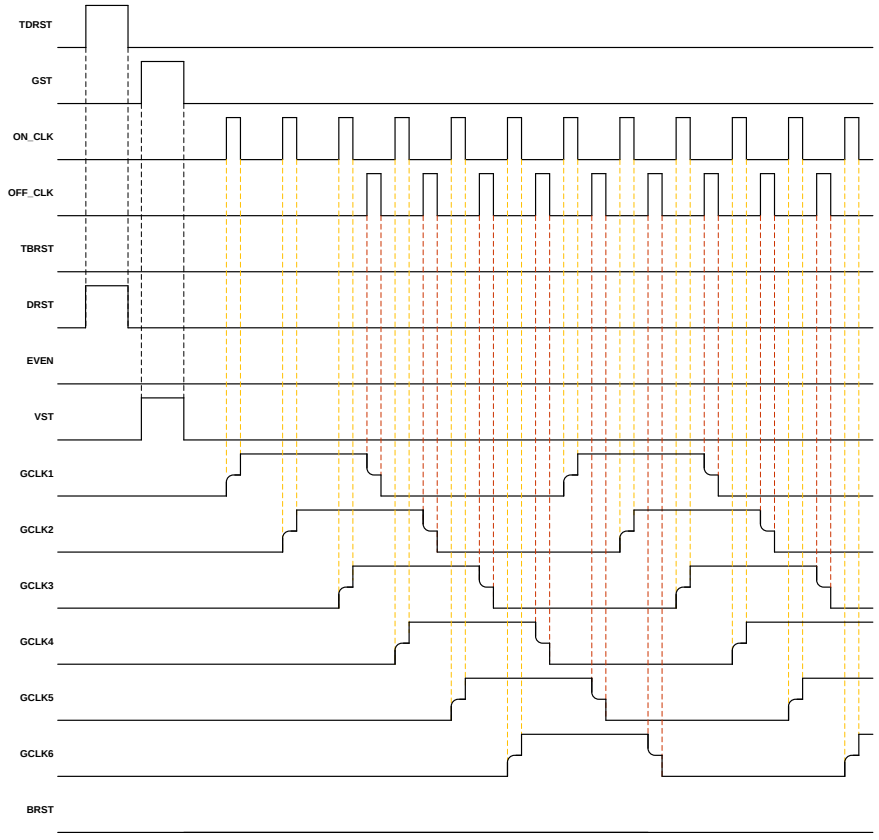



**Figure 5 ) Timing Diagram, Start of Frame**

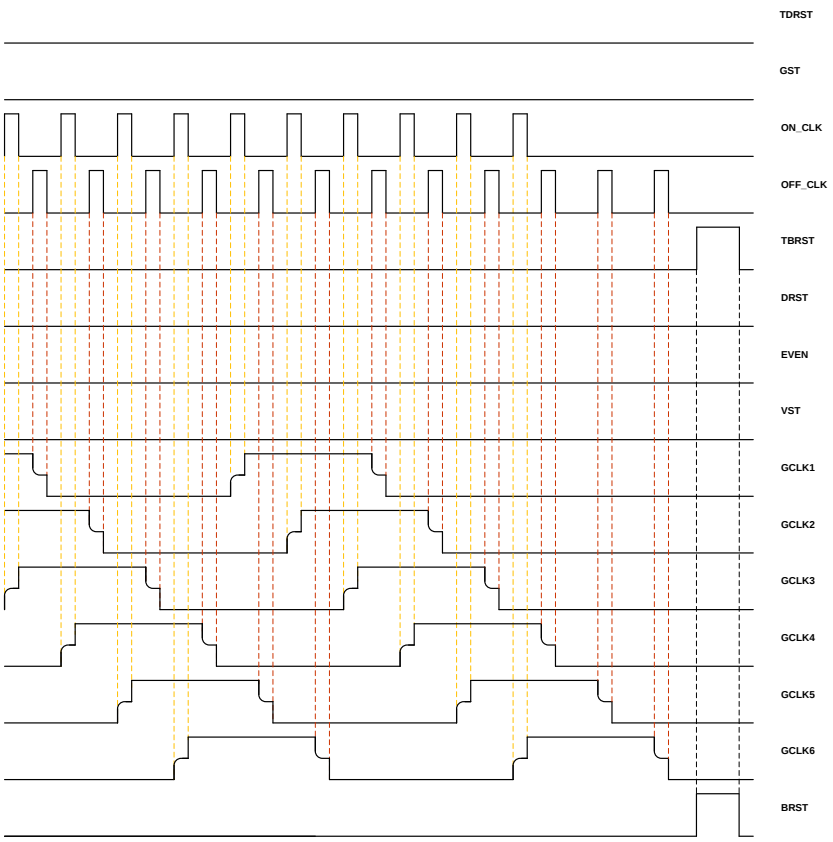
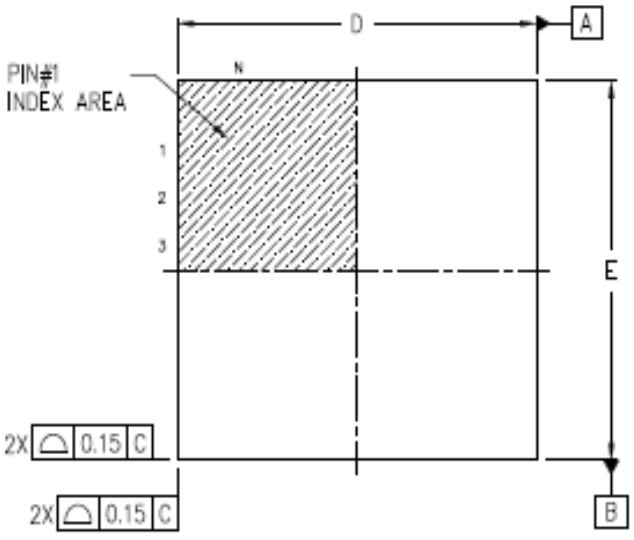
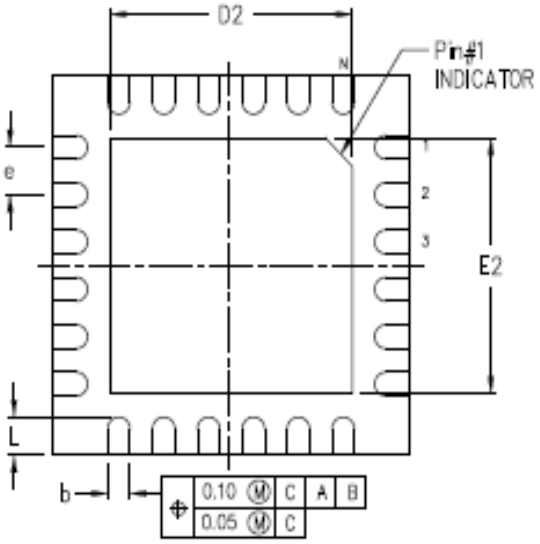



**Figure 6 ) Timing Diagram, End of Frame**

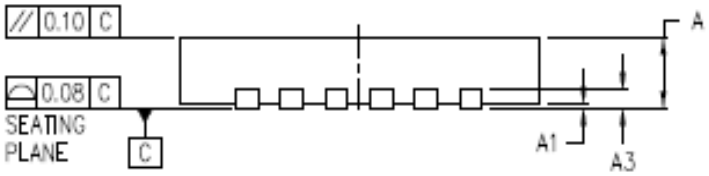
## Package Dimensions




TOP VIEW




BOTTOM VIEW




SIDE VIEW

| Symbol | Dimension (mm) | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| D | 3.85 | 4.00 | 4.15 |
| E | 3.85 | 4.00 | 4.15 |
| D2 | 2.60 | 2.70 | 2.80 |
| E2 | 2.60 | 2.70 | 2.80 |
| b | 0.18 | 0.25 | 0.30 |
| e | | 0.50 BSC | |
| L | 0.30 | 0.40 | 0.50 |

## REVISION HISTORY

| Date | Version | Changes |
|---|---|---|
| 2014-12-05 | Version 0.0 | Initial Version |
| 2015-02-12 | Version 0.1 | Update the description |
| 2015-09-01 | Version 0.2 | Mode 2 Option Cancel<br>Package POD update<br>VIH Threshold voltage level change |
| 2015-11-04 | Version 0.3 | Update Absolute Maximum Rate |
| 2016-01-19 | Version 0.4 | Update Pin Description ( Option → NC ) |
| 2016-05-27 | Version 1.0 | Update Final Datasheet |
| 2016-06-10 | Version 1.1 | Update Power Sequence<br>Update Package Dimension Format<br>Update BOM File |